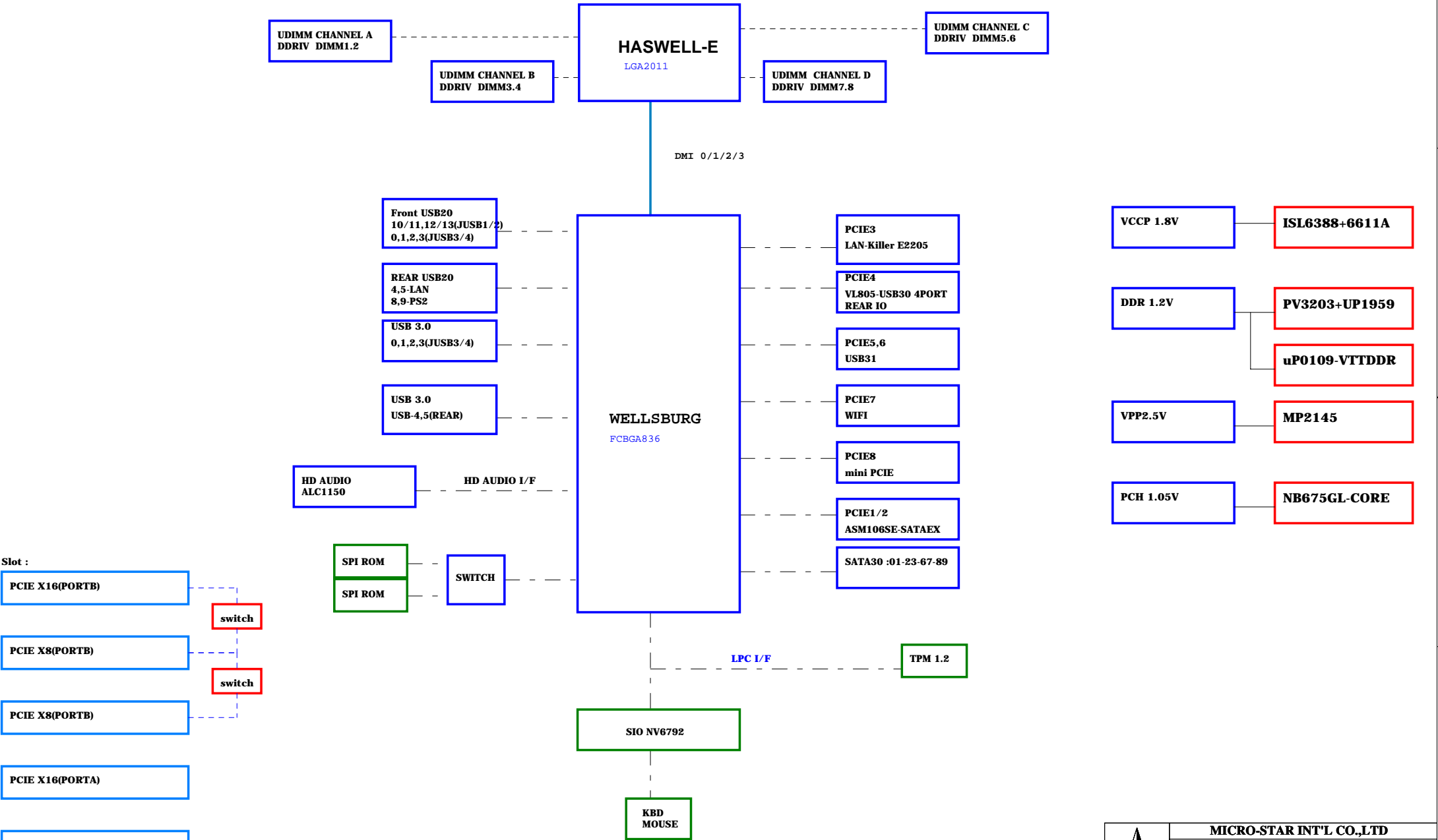


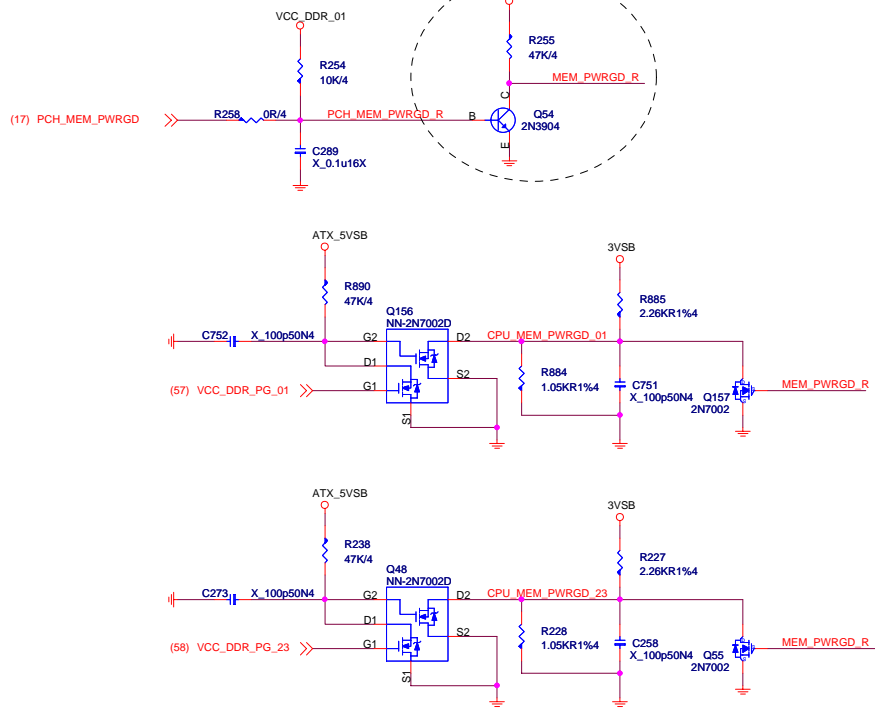
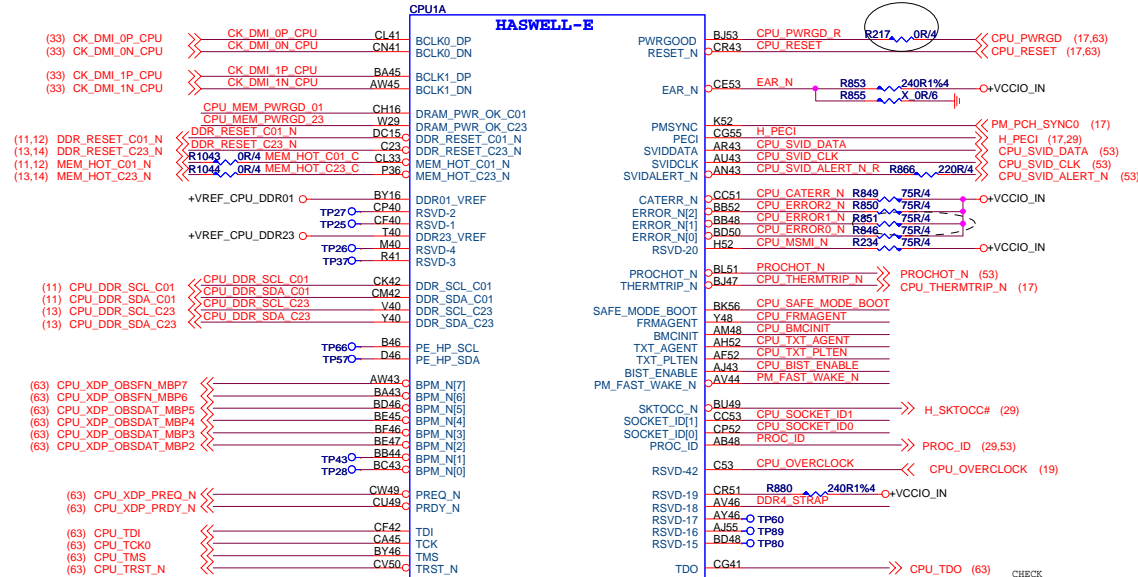


MS-7882 Block Diagram

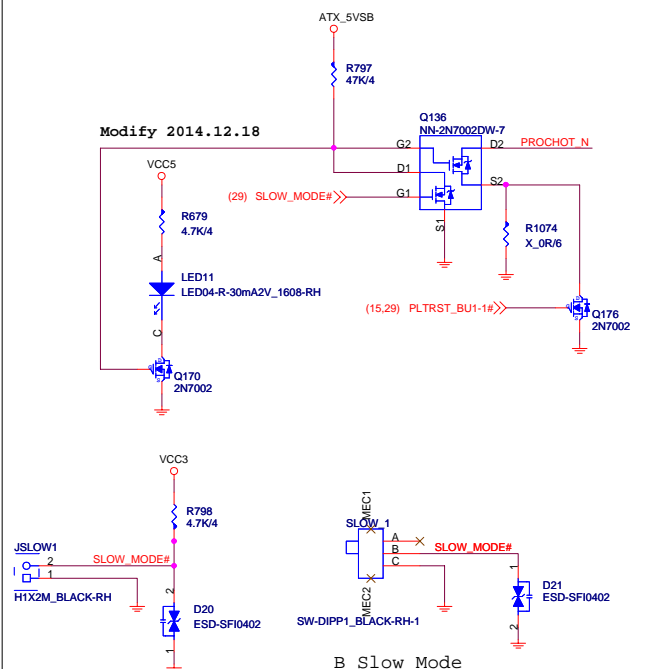


# CPU-CLK/Control/MISC

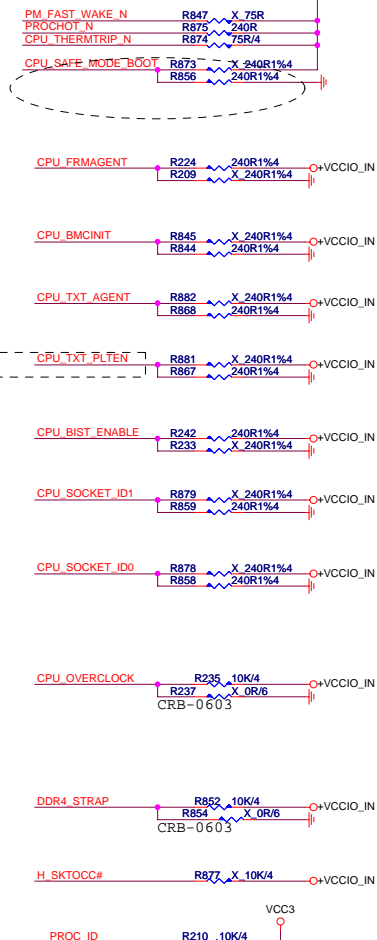
OR:R278 REMOVED



## slow mode circuit



Modify R875 2015.01.05



PROC_ID	+VCCIO_IN
0	0.95V
1	1.05V

## CPU-DMI / PEG

## CPU1F

## HASWELL-E

(18) DMI_RX3	DMI_RX3	C248	0.1u/10X4 DMI CPU RX3	E47	DMI_RX_DP[3]	D42	DMI CPU TX3	C252	0.1u/10X4 DMI TX3	>>DMI_TX3 (18)
(18) DMI_RX2	DMI_RX2	C265	0.1u/10X4 DMI CPU RX2	D48	DMI_RX_DP[2]	E43	DMI CPU TX2	C268	0.1u/10X4 DMI TX2	>>DMI_TX2 (18)
(18) DMI_RX1	DMI_RX1	C246	0.1u/10X4 DMI CPU RX1	E49	DMI_RX_DP[1]	D44	DMI CPU TX1	C259	0.1u/10X4 DMI TX1	>>DMI_TX1 (18)
(18) DMI_RX0	DMI_RX0	C263	0.1u/10X4 DMI CPU RX0	D50	DMI_RX_DP[0]	E45	DMI CPU TX0	C267	0.1u/10X4 DMI TX0	>>DMI_TX0 (18)
(18) DMI_RX3#	DMI_RX3#	C249	0.1u/10X4 DMI CPU RX3#	C47	DMI_RX_DN[3]	B42	DMI CPU TX3#	C253	0.1u/10X4 DMI TX3#	>>DMI_TX3# (18)
(18) DMI_RX2#	DMI_RX2#	C266	0.1u/10X4 DMI CPU RX2#	B48	DMI_RX_DN[2]	C43	DMI CPU TX2#	C270	0.1u/10X4 DMI TX2#	>>DMI_TX2# (18)
(18) DMI_RX1#	DMI_RX1#	C247	0.1u/10X4 DMI CPU RX1#	C49	DMI_RX_DN[1]	B44	DMI CPU TX1#	C251	0.1u/10X4 DMI TX1#	>>DMI_TX1# (18)
(18) DMI_RX0#	DMI_RX0#	C264	0.1u/10X4 DMI CPU RX0#	B50	DMI_RX_DN[0]	C45	DMI CPU TX0#	C268	0.1u/10X4 DMI TX0#	>>DMI_TX0# (18)
(48) EXP_C_RXP_7				M56	PE1B_RX_DP[7]	L49			>>EXP_C_TXP_7 (48)	
(48) EXP_C_RXP_6				L57	PE1B_RX_DP[6]	K48			>>EXP_C_TXP_6 (48)	
(48) EXP_C_RXP_5				M54	PE1B_RX_DP[5]	L47			>>EXP_C_TXP_5 (48)	
(48) EXP_C_RXP_4				L53	PE1B_RX_DP[4]	K46			>>EXP_C_TXP_4 (48)	
(48) EXP_C_RXN_7				K56	PE1B_RX_DN[7]	J49			>>EXP_C_TXN_7 (48)	
(48) EXP_C_RXN_6				J57	PE1B_RX_DN[6]	H48			>>EXP_C_TXN_6 (48)	
(48) EXP_C_RXN_5				K54	PE1B_RX_DN[5]	J47			>>EXP_C_TXN_5 (48)	
(48) EXP_C_RXN_4				J53	PE1B_RX_DN[4]	H46			>>EXP_C_TXN_4 (48)	
(28) EXP_C_RXP_3				G55	PE1A_RX_DP[3]	L45			>>EXP_C_TXP_3 (28)	
(28) EXP_C_RXP_2				F54	PE1A_RX_DP[2]	K44			>>EXP_C_TXP_2 (28)	
(28) EXP_C_RXP_1				F52	PE1A_RX_DP[1]	L43			>>EXP_C_TXP_1 (28)	
(28) EXP_C_RXP_0				F51	PE1A_RX_DP[0]	K42			>>EXP_C_TXP_0 (28)	
(28) EXP_C_RXN_3				E55	PE1A_RX_DN[3]	L45			>>EXP_C_TXN_3 (28)	
(28) EXP_C_RXN_2				D54	PE1A_RX_DN[2]	H44			>>EXP_C_TXN_2 (28)	
(28) EXP_C_RXN_1				D52	PE1A_RX_DN[1]	J43			>>EXP_C_TXN_1 (28)	
(28) EXP_C_RXN_0				C51	PE1A_RX_DN[0]	H42			>>EXP_C_TXN_0 (28)	
Not functional in HSW-E 28-lane SKU										
(27) EXP_A_RXP_15				BB56	PE2D_RX_DP[15]	BA47			>>EXP_A_TXP_15 (27)	
(27) EXP_A_RXP_14				BA57	PE2D_RX_DP[14]	AY48			>>EXP_A_TXP_14 (27)	
(27) EXP_A_RXP_13				AT56	PE2D_RX_DP[13]	BA49			>>EXP_A_TXP_13 (27)	
(27) EXP_A_RXP_12				AV58	PE2D_RX_DP[12]	AY50			>>EXP_A_TXP_12 (27)	
(27) EXP_A_RXN_15				AY56	PE2D_RX_DN[15]	AW47			>>EXP_A_TXN_15 (27)	
(27) EXP_A_RXN_14				AY58	PE2D_RX_DN[14]	AV48			>>EXP_A_TXN_14 (27)	
(27) EXP_A_RXN_13				AP56	PE2D_RX_DN[13]	AW49			>>EXP_A_TXN_13 (27)	
(27) EXP_A_RXN_12				AT58	PE2D_RX_DN[12]	AV50			>>EXP_A_TXN_12 (27)	
(27) EXP_A_RXP_11				AU57	PE2C_RX_DP[11]	BA51			>>EXP_A_TXP_11 (27)	
(27) EXP_A_RXP_10				AL57	PE2C_RX_DP[10]	BB54			>>EXP_A_TXP_10 (27)	
(27) EXP_A_RXP_9				AM58	PE2C_RX_DP[9]	BA53			>>EXP_A_TXP_9 (27)	
(27) EXP_A_RXP_8				AK56	PE2C_RX_DP[8]	AY52			>>EXP_A_TXP_8 (27)	
(27) EXP_A_RXN_11				AR57	PE2C_RX_DN[11]	AW51			>>EXP_A_TXN_11 (27)	
(27) EXP_A_RXN_10				AJ57	PE2C_RX_DN[10]	AY54			>>EXP_A_TXN_10 (27)	
(27) EXP_A_RXN_9				AK58	PE2C_RX_DN[9]	AW53			>>EXP_A_TXN_9 (27)	
(27) EXP_A_RXN_8				AH56	PE2C_RX_DN[8]	AY52			>>EXP_A_TXN_8 (27)	
(27) EXP_A_RXP_7				AF58	PE2B_RX_DP[7]	AT54			>>EXP_A_TXP_7 (27)	
(27) EXP_A_RXP_6				AE55	PE2B_RX_DP[6]	AR53			>>EXP_A_TXP_6 (27)	
(27) EXP_A_RXP_5				AD56	PE2B_RX_DP[5]	AK54			>>EXP_A_TXP_5 (27)	
(27) EXP_A_RXP_4				AD54	PE2B_RX_DP[4]	AJ53			>>EXP_A_TXP_4 (27)	
(27) EXP_A_RXN_7				AE57	PE2B_RX_DN[7]	AP54			>>EXP_A_TXN_7 (27)	
(27) EXP_A_RXN_6				AC55	PE2B_RX_DN[6]	AN53			>>EXP_A_TXN_6 (27)	
(27) EXP_A_RXN_5				AB56	PE2B_RX_DN[5]	AH54			>>EXP_A_TXN_5 (27)	
(27) EXP_A_RXN_4				AB54	PE2B_RX_DN[4]	AG53			>>EXP_A_TXN_4 (27)	
(27) EXP_A_RXP_3				W55	PE2A_RX_DP[3]	AP52			>>EXP_A_TXP_3 (27)	
(27) EXP_A_RXP_2				V56	PE2A_RX_DP[2]	AR51			>>EXP_A_TXP_2 (27)	
(27) EXP_A_RXP_1				V54	PE2A_RX_DP[1]	AP50			>>EXP_A_TXP_1 (27)	
(27) EXP_A_RXP_0				N55	PE2A_RX_DP[0]	AR49			>>EXP_A_TXP_0 (27)	
(27) EXP_A_RXN_3				U55	PE2A_RX_DN[3]	AM52			>>EXP_A_TXN_3 (27)	
(27) EXP_A_RXN_2				T56	PE2A_RX_DN[2]	AN51			>>EXP_A_TXN_2 (27)	
(27) EXP_A_RXN_1				T54	PE2A_RX_DN[1]	AM50			>>EXP_A_TXN_1 (27)	
(27) EXP_A_RXN_0				L55	PE2A_RX_DN[0]	AN49			>>EXP_A_TXN_0 (27)	

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## CPU1G

## HASWELL-E

(24) EXP_B_RXP_15		AR45	PE3D_RX_DP[15]	P44	>>EXP_B_TXP_15 (24)
(24) EXP_B_RXP_14		AP46	PE3D_RX_DP[14]	AA43	>>EXP_B_TXP_14 (24)
(24) EXP_B_RXP_13		AR47	PE3D_RX_DP[13]	AB44	>>EXP_B_TXP_13 (24)
(24) EXP_B_RXP_12		AJ47	PE3D_RX_DP[12]	AC45	>>EXP_B_TXP_12 (24)
(24) EXP_B_RXN_15		AN45	PE3D_RX_DN[15]	T44	>>EXP_B_TXN_15 (24)
(24) EXP_B_RXN_14		AM46	PE3D_RX_DN[14]	AC43	>>EXP_B_TXN_14 (24)
(24) EXP_B_RXN_13		AN47	PE3D_RX_DN[13]	Y44	>>EXP_B_TXN_13 (24)
(24) EXP_B_RXN_12		AG47	PE3D_RX_DN[12]	AA45	>>EXP_B_TXN_12 (24)
(24) EXP_B_RXP_11		AJ49	PE3C_RX_DP[11]	AB46	>>EXP_B_TXP_11 (24)
(24) EXP_B_RXP_10		AH50	PE3C_RX_DP[10]	AC47	>>EXP_B_TXP_10 (24)
(24) EXP_B_RXP_9		AJ51	PE3C_RX_DP[9]	U45	>>EXP_B_TXP_9 (24)
(24) EXP_B_RXP_8		AH48	PE3C_RX_DP[8]	T46	>>EXP_B_TXP_8 (24)
(24) EXP_B_RXN_11		AG49	PE3C_RX_DN[11]	Y46	>>EXP_B_TXN_11 (24)
(24) EXP_B_RXN_10		AF50	PE3C_RX_DN[10]	AA47	>>EXP_B_TXN_10 (24)
(24) EXP_B_RXN_9		AG51	PE3C_RX_DN[9]	R45	>>EXP_B_TXN_9 (24)
(24) EXP_B_RXN_8		AF48	PE3C_RX_DN[8]	P46	>>EXP_B_TXN_8 (24)
(25) EXP_B_RXP_7		AC51	PE3B_RX_DP[7]	U49	>>EXP_B_TXP_7 (25)
(25) EXP_B_RXP_6		AC53	PE3B_RX_DP[6]	T50	>>EXP_B_TXP_6 (25)
(25) EXP_B_RXP_5		AB52	PE3B_RX_DP[5]	U51	>>EXP_B_TXP_5 (25)
(25) EXP_B_RXP_4		AB50	PE3B_RX_DP[4]	T52	>>EXP_B_TXP_4 (25)
(25) EXP_B_RXN_7		AA51	PE3B_RX_DN[7]	R49	>>EXP_B_TXN_7 (25)
(25) EXP_B_RXN_6		AA53	PE3B_RX_DN[6]	P50	>>EXP_B_TXN_6 (25)
(25) EXP_B_RXN_5		Y52	PE3B_RX_DN[5]	R51	>>EXP_B_TXN_5 (25)
(25) EXP_B_RXN_4		Y50	PE3B_RX_DN[4]	P52	>>EXP_B_TXN_4 (25)
(25) EXP_B_RXP_3		AC49	PE3A_RX_DP[3]	T48	>>EXP_B_TXP_3 (25)
(25) EXP_B_RXP_2		AH46	PE3A_RX_DP[2]	U47	>>EXP_B_TXP_2 (25)
(25) EXP_B_RXP_1		AJ45	PE3A_RX_DP[1]	L51	>>EXP_B_TXP_1 (25)
(25) EXP_B_RXP_0		AH44	PE3A_RX_DP[0]	K50	>>EXP_B_TXP_0 (25)
(25) EXP_B_RXN_3		AA49	PE3A_RX_DN[3]	P48	>>EXP_B_TXN_3 (25)
(25) EXP_B_RXN_2		AF46	PE3A_RX_DN[2]	R47	>>EXP_B_TXN_2 (25)
(25) EXP_B_RXN_1		AG45	PE3A_RX_DN[1]	J51	>>EXP_B_TXN_1 (25)
(25) EXP_B_RXN_0		AF44	PE3A_RX_DN[0]	H50	>>EXP_B_TXN_0 (25)

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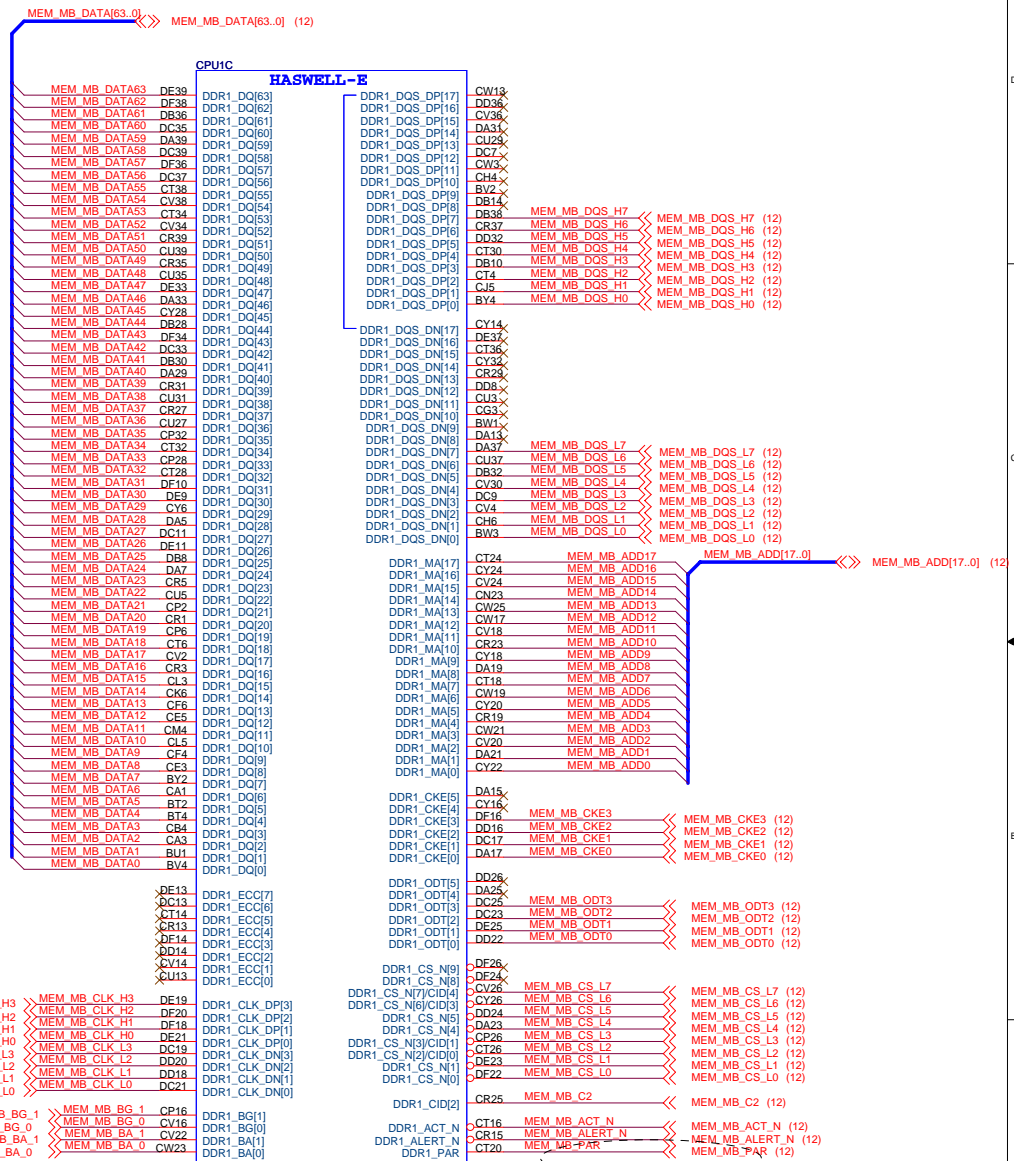
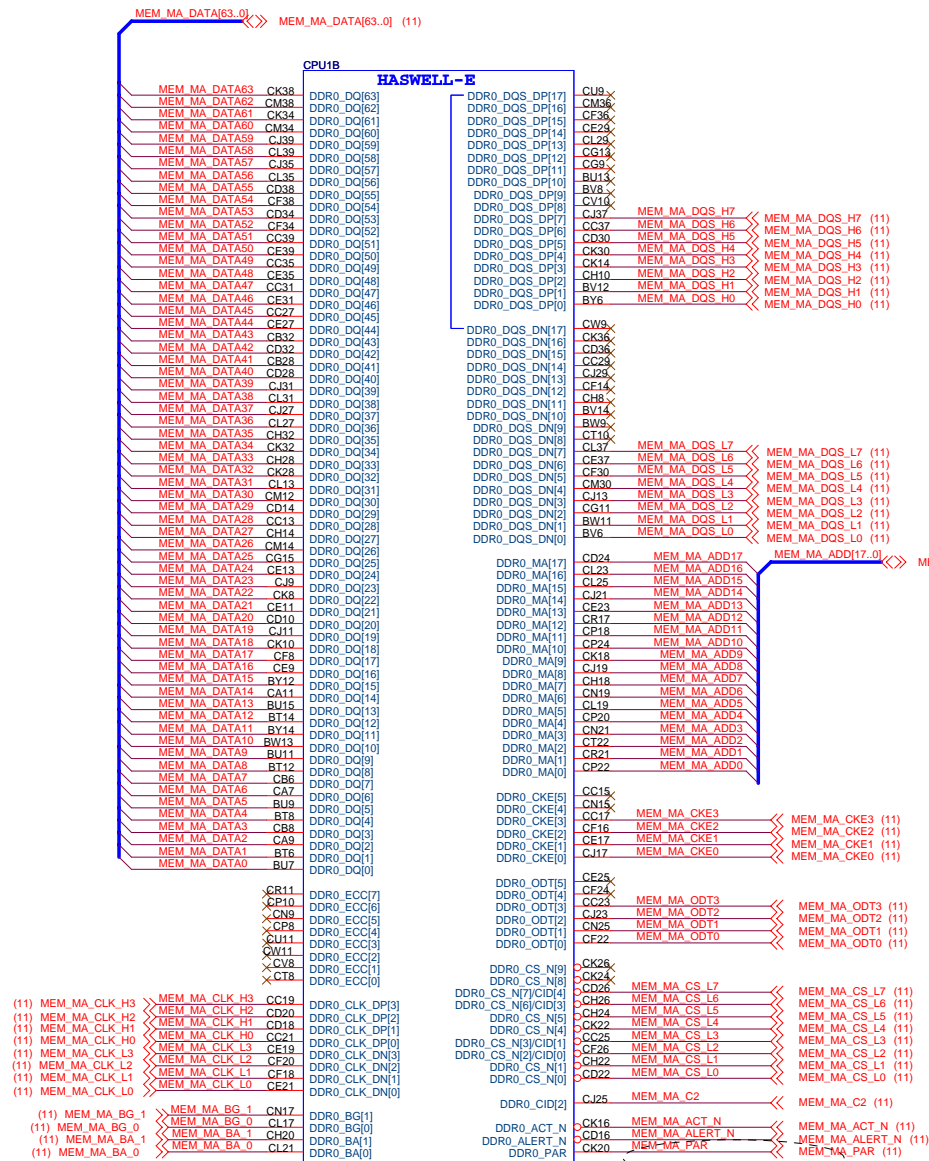


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Size Custom	Document Description CPU-DMI/PEG	Rev 2.0
Date: Monday, January 12, 2015		Sheet 4 of 67

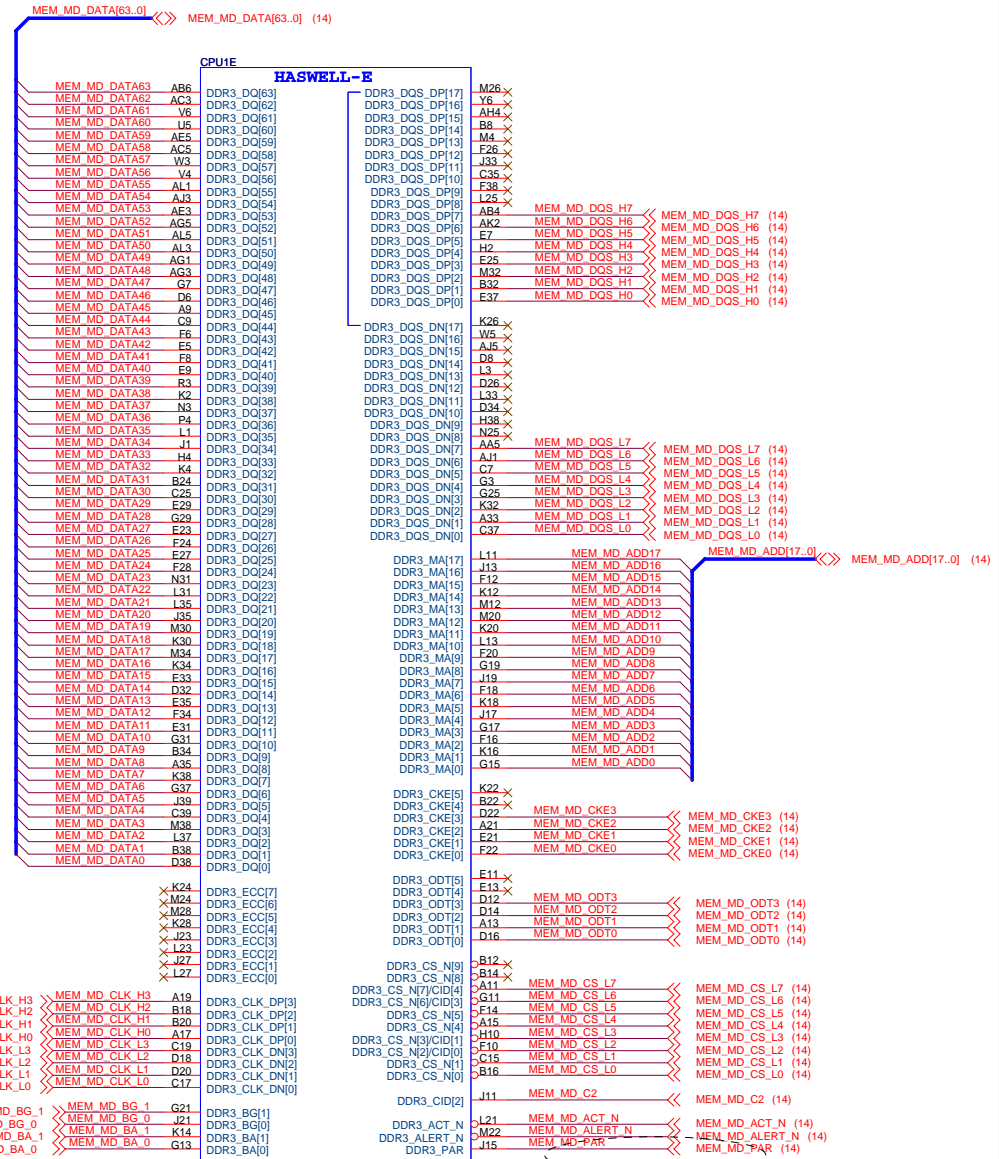
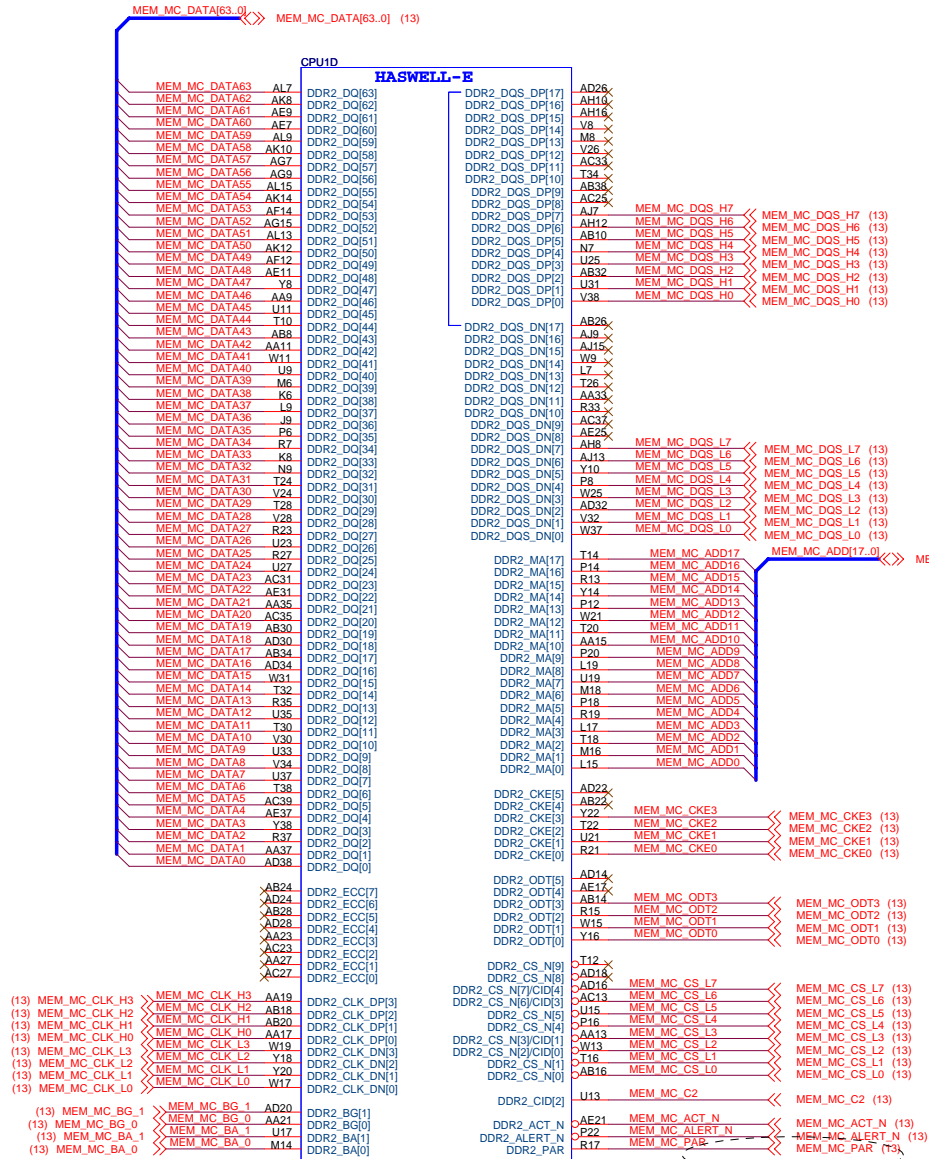
## CPU-Memory0/1



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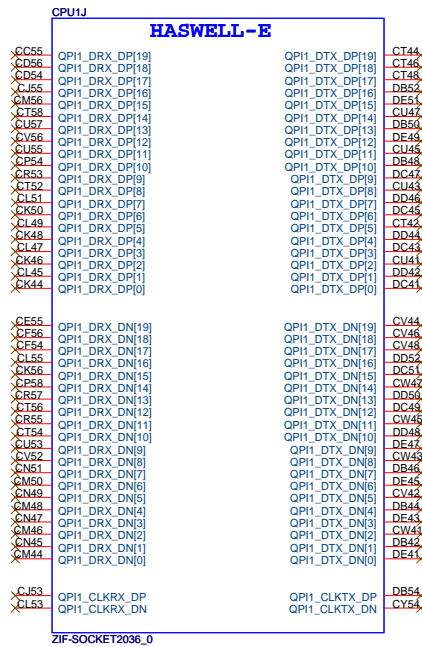
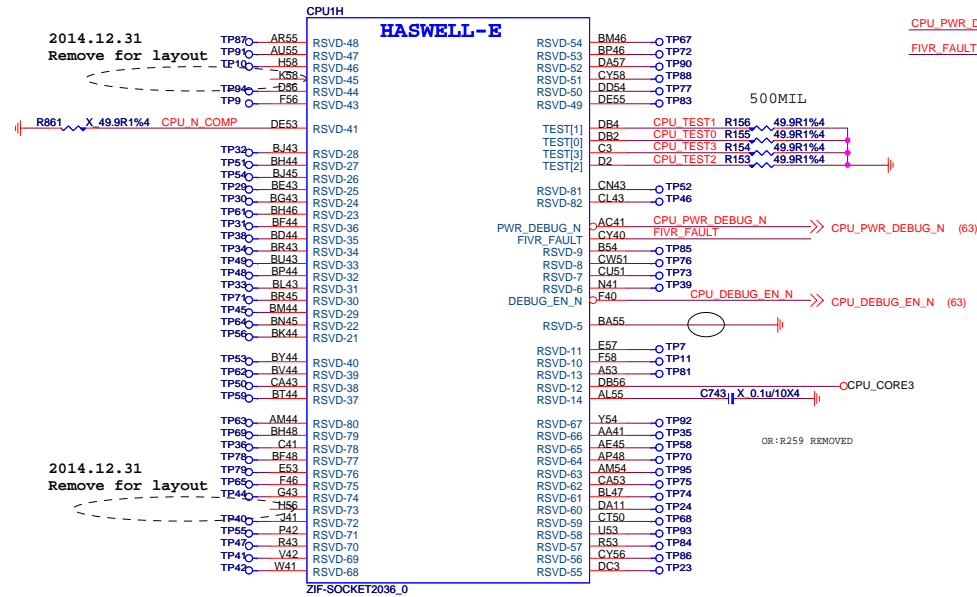
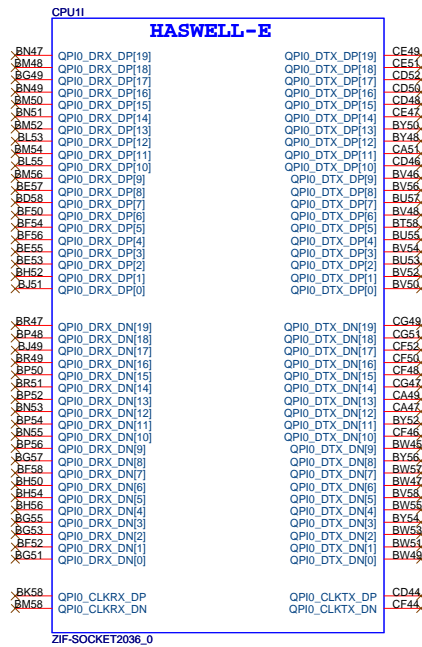
## CPU-Memory2/3



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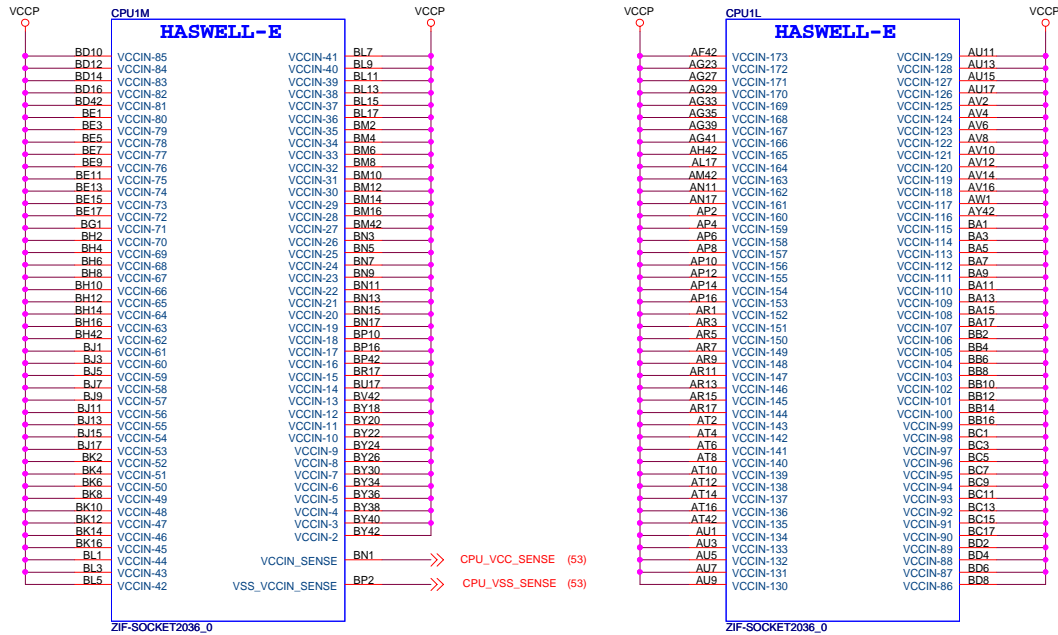


MICRO-STAR INT'L CO.,LTD

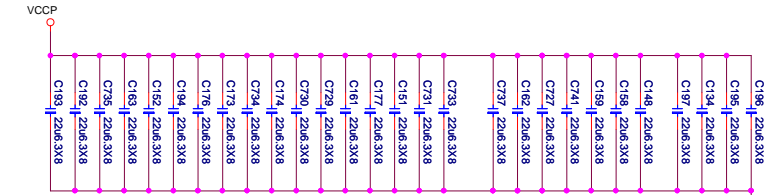
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Size Custom	Document Description CPU-QPI/RESERVE	Rev 2.0
Date: Monday, January 12, 2015		Sheet 7 of 67

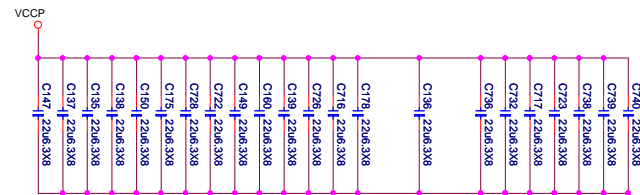
# CPU-Power



## +CPU\_VCCP-Decoupling



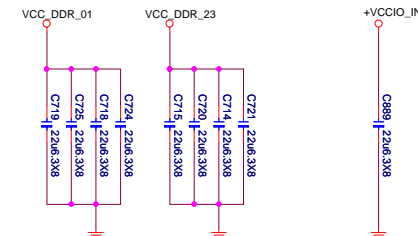
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY



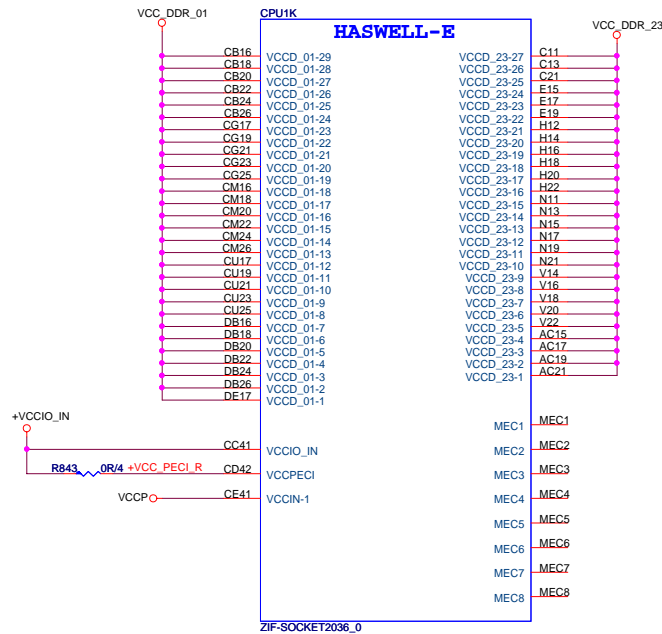
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

Skt cavity caps, place: 28 on top side & 26 on back side.

## +CPU\_DDR-Decoupling



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY





## CPU1N

## HASWELL-E

A23	VSS-629	M2	VSS-553	M36	VSS-472
A37	VSS-628	M36	VSS-551	M42	VSS-480
A39	VSS-627	M42	VSS-550	M44	VSS-471
A41	VSS-626	M44	VSS-549	M46	VSS-470
A43	VSS-625	M46	VSS-548	M48	VSS-469
A45	VSS-624	M48	VSS-547	M50	VSS-467
A47	VSS-623	M50	VSS-546	M52	VSS-466
A49	VSS-622	M52	VSS-545	M54	VSS-468
A5	VSS-631	M54	VSS-543	M56	VSS-465
A51	VSS-621	M56	VSS-542	M58	VSS-464
A7	VSS-630	M58	VSS-541	M60	VSS-463
B10	VSS-619	M60	VSS-540	M62	VSS-462
B36	VSS-618	M62	VSS-539	M64	VSS-461
B40	VSS-617	M64	VSS-538	M66	VSS-460
B52	VSS-616	M66	VSS-537	M68	VSS-459
B6	VSS-620	M68	VSS-536	M70	VSS-458
C33	VSS-614	M70	VSS-535	M72	VSS-457
C5	VSS-615	M72	VSS-534	M74	VSS-456
C55	VSS-613	M74	VSS-533	M76	VSS-455
D10	VSS-611	M76	VSS-532	M78	VSS-454
D24	VSS-610	M78	VSS-531	M80	VSS-453
D36	VSS-609	M80	VSS-530	M82	VSS-451
D4	VSS-612	M82	VSS-529	M84	VSS-450
D40	VSS-608	M84	VSS-528	M86	VSS-449
E1	VSS-607	M86	VSS-527	M88	VSS-448
E3	VSS-606	M88	VSS-526	M90	VSS-447
E39	VSS-605	M90	VSS-525	M92	VSS-446
E41	VSS-604	M92	VSS-524	M94	VSS-445
F2	VSS-603	M94	VSS-523	M96	VSS-444
F30	VSS-601	M96	VSS-522	M98	VSS-443
F32	VSS-600	M98	VSS-521	M100	VSS-442
F36	VSS-599	M100	VSS-520	M102	VSS-441
F4	VSS-598	M102	VSS-519	M104	VSS-440
F42	VSS-597	M104	VSS-518	M106	VSS-439
F44	VSS-596	M106	VSS-517	M108	VSS-438
F48	VSS-595	M108	VSS-516	M110	VSS-437
F50	VSS-594	M110	VSS-515	M112	VSS-436
G1	VSS-593	M112	VSS-514	M114	VSS-435
G23	VSS-591	M114	VSS-513	M116	VSS-434
G27	VSS-590	M116	VSS-512	M118	VSS-433
G33	VSS-589	M118	VSS-511	M120	VSS-432
G35	VSS-588	M120	VSS-510	M122	VSS-431
G39	VSS-587	M122	VSS-509	M124	VSS-430
G41	VSS-586	M124	VSS-508	M126	VSS-429
G45	VSS-585	M126	VSS-507	M128	VSS-428
G47	VSS-584	M128	VSS-506	M130	VSS-427
G49	VSS-583	M130	VSS-505	M132	VSS-426
G5	VSS-593	M132	VSS-504	M134	VSS-425
G51	VSS-592	M134	VSS-503	M136	VSS-424
G53	VSS-591	M136	VSS-502	M138	VSS-423
G57	VSS-590	M138	VSS-501	M140	VSS-422
G9	VSS-589	M140	VSS-500	M142	VSS-421
H24	VSS-577	M142	VSS-499	M144	VSS-420
H26	VSS-576	M144	VSS-498	M146	VSS-419
H28	VSS-575	M146	VSS-497	M148	VSS-418
H30	VSS-574	M148	VSS-496	M150	VSS-417
H32	VSS-573	M150	VSS-495	M152	VSS-416
H34	VSS-572	M152	VSS-494	M154	VSS-415
H36	VSS-571	M154	VSS-493	M156	VSS-414
H40	VSS-570	M156	VSS-492	M158	VSS-413
H54	VSS-569	M158	VSS-491	M160	VSS-412
H6	VSS-579	M160	VSS-490	M162	VSS-411
H8	VSS-578	M162	VSS-489	M164	VSS-410
J25	VSS-565	M164	VSS-488	M166	VSS-409
J29	VSS-564	M166	VSS-487	M168	VSS-408
J3	VSS-563	M168	VSS-486	M170	VSS-407
J31	VSS-562	M170	VSS-485	M172	VSS-406
J37	VSS-561	M172	VSS-484	M174	VSS-405
J5	VSS-560	M174	VSS-483	M176	VSS-404
J53	VSS-559	M176	VSS-482	M178	VSS-403
J7	VSS-558	M178	VSS-481	M180	VSS-402
K10	VSS-557	M180	VSS-480	M182	VSS-401
K36	VSS-556	M182	VSS-479	M184	VSS-400
K40	VSS-555	M184	VSS-478	M186	VSS-399
L29	VSS-554	M186	VSS-477	M188	VSS-398
L39	VSS-553	M188	VSS-476	M190	VSS-397
L41	VSS-552	M190	VSS-475	M192	VSS-396
L5	VSS-551	M192	VSS-474	M194	VSS-395
M10	VSS-550	M194	VSS-473	M196	VSS-394

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## CPU1O

## HASWELL-E

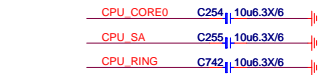
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Y4	VSS-480	AH14	VSS-393	AH16	VSS-392
Y42	VSS-471	AH16	VSS-392	AH18	VSS-391
Y56	VSS-470	AH18	VSS-391	AH20	VSS-390
AA3	VSS-469	AH20	VSS-390	AH22	VSS-389
AA25	VSS-467	AH22	VSS-389	AH24	VSS-388
AA29	VSS-466	AH24	VSS-388	AH26	VSS-387
AA7	VSS-468	AH26	VSS-387	AH28	VSS-386
AA31	VSS-465	AH28	VSS-386	AH30	VSS-385
AA39	VSS-464	AH30	VSS-385	AH32	VSS-384
AA55	VSS-463	AH32	VSS-384	AH34	VSS-383
AB12	VSS-462	AH34	VSS-383	AH36	VSS-382
AB36	VSS-461	AH36	VSS-382	AH38	VSS-381
AB40	VSS-460	AH38	VSS-381	AH40	VSS-380
AB42	VSS-459	AH40	VSS-380	AH42	VSS-379
AC7	VSS-458	AH42	VSS-379	AH44	VSS-378
AC9	VSS-457	AH44	VSS-378	AH46	VSS-377
AC11	VSS-456	AH46	VSS-377	AH48	VSS-376
AC29	VSS-455	AH48	VSS-376	AH50	VSS-375
AD4	VSS-454	AH50	VSS-375	AH52	VSS-374
AD8	VSS-453	AH52	VSS-374	AH54	VSS-373
AD6	VSS-451	AH54	VSS-373	AH56	VSS-372
AD10	VSS-450	AH56	VSS-372	AH58	VSS-371
AD12	VSS-449	AH58	VSS-371	AH60	VSS-370
AD40	VSS-448	AH60	VSS-370	AH62	VSS-369
AD42	VSS-447	AH62	VSS-369	AH64	VSS-368
AD44	VSS-446	AH64	VSS-368	AH66	VSS-367
AD46	VSS-445	AH66	VSS-367	AH68	VSS-366
AD48	VSS-444	AH68	VSS-366	AH70	VSS-365
AD50	VSS-443	AH70	VSS-365	AH72	VSS-364
AD52	VSS-442	AH72	VSS-364	AH74	VSS-363
AE13	VSS-441	AH74	VSS-363	AH76	VSS-362
AE15	VSS-440	AH76	VSS-362	AH78	VSS-361
AE19	VSS-439	AH78	VSS-361	AH80	VSS-360
AE23	VSS-438	AH80	VSS-360	AH82	VSS-359
AE27	VSS-437	AH82	VSS-359	AH84	VSS-358
AE29	VSS-436	AH84	VSS-358	AH86	VSS-357
AE33	VSS-435	AH86	VSS-357	AH88	VSS-356
AE35	VSS-434	AH88	VSS-356	AH90	VSS-355
AE39	VSS-433	AH90	VSS-355	AH92	VSS-354
AE41	VSS-432	AH92	VSS-354	AH94	VSS-353
AE43	VSS-431	AH94	VSS-353	AH96	VSS-352
AE47	VSS-430	AH96	VSS-352	AH98	VSS-351
AE49	VSS-429	AH98	VSS-351	AH100	VSS-350
AF10	VSS-428	AH100	VSS-350	AH102	VSS-349
AF16	VSS-427	AH102	VSS-349	AH104	VSS-348
AF18	VSS-426	AH104	VSS-348	AH106	VSS-347
AF51	VSS-425	AH106	VSS-347	AH108	VSS-346
AE53	VSS-424	AH108	VSS-346	AH110	VSS-345
AF2	VSS-423	AH110	VSS-345	AH112	VSS-344
AF4	VSS-422	AH112	VSS-344	AH114	VSS-343
AF6	VSS-421	AH114	VSS-343	AH116	VSS-342
AF8	VSS-420	AH116	VSS-342	AH118	VSS-341
AF20	VSS-419	AH118	VSS-341	AH120	VSS-340
AF22	VSS-418	AH120	VSS-340	AH122	VSS-339
AF24	VSS-417	AH122	VSS-339	AH124	VSS-338
AF26	VSS-416	AH124	VSS-338	AH126	VSS-337
AF28	VSS-415	AH126	VSS-337	AH128	VSS-336
AF30	VSS-414	AH128	VSS-336	AH130	VSS-335
AF32	VSS-413	AH130	VSS-335	AH132	VSS-334
AF34	VSS-412	AH132	VSS-334	AH134	VSS-333
AF36	VSS-411	AH134	VSS-333	AH136	VSS-332
AF38	VSS-410	AH136	VSS-332	AH138	VSS-331
AF40	VSS-409	AH138	VSS-331	AH140	VSS-330
AF54	VSS-408	AH140	VSS-330	AH142	VSS-329
AF56	VSS-407	AH142	VSS-329	AH144	VSS-328
AG11	VSS-406	AH144	VSS-328	AH146	VSS-327
AG13	VSS-405	AH146	VSS-327	AH148	VSS-326
AG17	VSS-404	AH148	VSS-326	AH150	VSS-325
AG19	VSS-403	AH150	VSS-325	AH152	VSS-324
AG21	VSS-402	AH152	VSS-324	AH154	VSS-323
AG25	VSS-401	AH154	VSS-323	AH156	VSS-322
AG31	VSS-400	AH156	VSS-322	AH158	VSS-321
AG37	VSS-399	AH158	VSS-321	AH160	VSS-320
AG43	VSS-398	AH160	VSS-320	AH162	VSS-319
AG55	VSS-397	AH162	VSS-319	AH164	VSS-318
AG57	VSS-396	AH164	VSS-318	AH166	VSS-317
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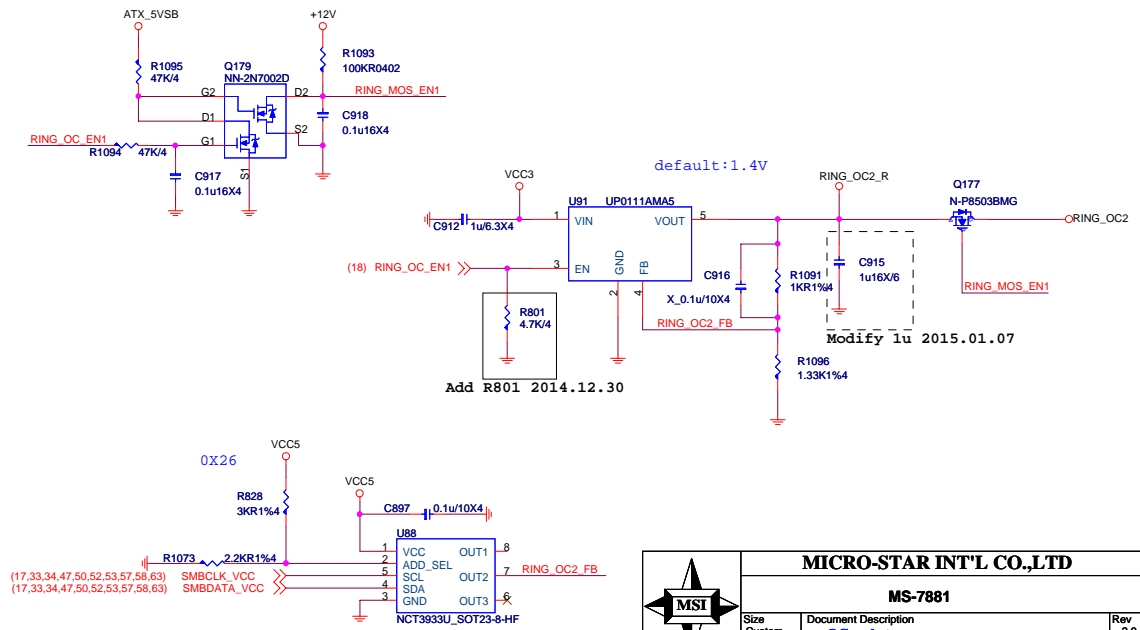
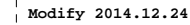
## CPU1P

## HASWELL-E

BC47	VSS-315	BW15	VSS-236	BW17	VSS-235
BC49	VSS-314	BW17	VSS-235	BW43	VSS-234
BC51	VSS-313	BW43	VSS-234	BW45	VSS-233
BC53	VSS-312	BW45	VSS-233	BW47	VSS-232
BC55	VSS-311	BW47	VSS-232	BW49	VSS-231
BC57	VSS-310	BW49	VSS-231	BW51	VSS-230
BD52	VSS-309	BW51	VSS-230	BW53	VSS-229
BD54	VSS-308	BW53	VSS-229	BW55	VSS-228
BD56	VSS-307	BW55	VSS-228	BW57	VSS-227
BE49	VSS-306	BW57	VSS-227	BW59	VSS-226
BE51	VSS-305	BW59	VSS-226	BW61	VSS-225
BF2	VSS-304	BW61	VSS-225	BW63	VSS-224
BF4	VSS-303	BW63	VSS-224	BW65	VSS-223
BF10	VSS-302	BW65	VSS-223	BW67	VSS-222
BF12	VSS-301	BW67	VSS-222	BW69	VSS-221
BF14	VSS-298	BW69	VSS-221	BW71	VSS-220
BF16	VSS-297	BW71	VSS-220	BW73	VSS-219
BF6	VSS-296	BW73	VSS-219	BW75	VSS-218
BF8	VSS-295	BW75	VSS-218	BW77	VSS-217
BF42	VSS-294	BW77	VSS-217	BW79	VSS-216
BG3	VSS-293	BW79	VSS-216	BW81	VSS-215
BG5	VSS-292	BW81	VSS-215	BW83	VSS-214
BG7	VSS-291	BW83	VSS-214	BW85	VSS-213
BG9	VSS-290	BW85	VSS-213	BW87	VSS-212
BG11	VSS-289	BW87	VSS-212	BW89	VSS-211
BG13	VSS-288	BW89	VSS-211	BW91	VSS-210
BG15	VSS-287	BW91	VSS-210	BW93	VSS-209
BG17	VSS-286	BW93	VSS-209	BW95	VSS-208
BG45	VSS-285	BW95	VSS-208	BW97	VSS-207
BG47	VSS-284	BW97	VSS-207	BW99	VSS-206
BH58	VSS-283	BW99	VSS-206	BW101	VSS-205
BL55	VSS-282	BW101	VSS-205	BW103	VSS-204
BL57	VSS-281	BW103	VSS-204	BW105	VSS-203
BK42	VSS-280	BW105	VSS-203	BW107	VSS-202
BK46	VSS-279	BW107	VSS-202	BW109	VSS-201
BK50	VSS-278	BW109	VSS-201	BW111	VSS-200
BK52	VSS-277	BW111	VSS-200	BW113	VSS-199
BK54	VSS-276	BW113	VSS-199	BW115	VSS-198
BL45	VSS-275	BW115	VSS-198	BW117	VSS-197
BL49	VSS-274	BW117	VSS-197	BW119	VSS-196
BL57	VSS-273	BW119	VSS-196	BW121	VSS-195
BM43	VSS-272	BW121	VSS-195	BW123	VSS-194
BN57	VSS-271	BW123	VSS-194	BW125	VSS-193
BP4	VSS-270	BW125	VSS-193	BW127	VSS-192
BP6	VSS-269	BW127	VSS-192	BW129	VSS-191
BP8	VSS-268	BW129	VSS-191	BW131	VSS-190
BP12	VSS-267	BW131	VSS-190	BW133	VSS-189
BP14	VSS-266	BW133	VSS-189	BW135	VSS-188
BP58	VSS-265	BW135	VSS-188	BW137	VSS-187
BR1	VSS-264	BW137	VSS-187	BW139	VSS-186
BR3	VSS-263	BW139	VSS-186	BW141	VSS-185</

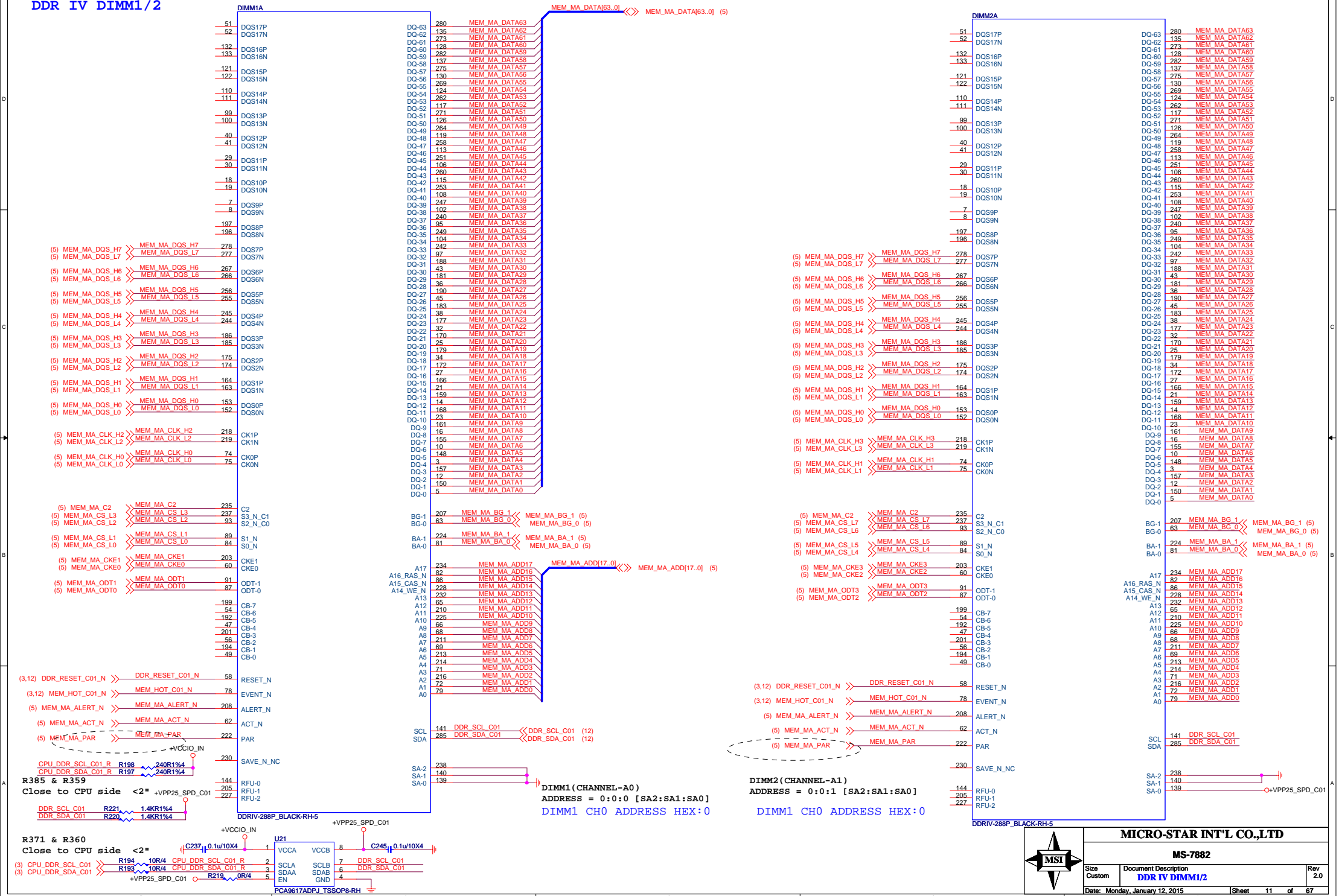


Remove DDR OC1~3 & RING OC1 circuit.



<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7881</b>			
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DDR IV DIMM1/2



## DDR IV DIMM3/4

DIMM3A

51 DQS17P  
52 DQS17N  
132 DQS16P  
133 DQS16N  
121 DQS15P  
122 DQS15N  
110 DQS14P  
111 DQS14N  
99 DQS13P  
100 DQS13N  
40 DQS12P  
41 DQS12N  
29 DQS11P  
30 DQS11N  
18 DQS10P  
19 DQS10N  
7 DQS9P  
8 DQS9N  
197 DQS8P  
196 DQS8N  
(5) MEM\_MB\_DQS\_H7 >> MEM\_MB\_DQS\_H7 278  
(5) MEM\_MB\_DQS\_L7 >> MEM\_MB\_DQS\_L7 277  
(5) MEM\_MB\_DQS\_H6 >> MEM\_MB\_DQS\_H6 267  
(5) MEM\_MB\_DQS\_L6 >> MEM\_MB\_DQS\_L6 266  
(5) MEM\_MB\_DQS\_H5 >> MEM\_MB\_DQS\_H5 256  
(5) MEM\_MB\_DQS\_L5 >> MEM\_MB\_DQS\_L5 255  
(5) MEM\_MB\_DQS\_H4 >> MEM\_MB\_DQS\_H4 245  
(5) MEM\_MB\_DQS\_L4 >> MEM\_MB\_DQS\_L4 244  
(5) MEM\_MB\_DQS\_H3 >> MEM\_MB\_DQS\_H3 186  
(5) MEM\_MB\_DQS\_L3 >> MEM\_MB\_DQS\_L3 185  
(5) MEM\_MB\_DQS\_H2 >> MEM\_MB\_DQS\_H2 175  
(5) MEM\_MB\_DQS\_L2 >> MEM\_MB\_DQS\_L2 174  
(5) MEM\_MB\_DQS\_H1 >> MEM\_MB\_DQS\_H1 164  
(5) MEM\_MB\_DQS\_L1 >> MEM\_MB\_DQS\_L1 163  
(5) MEM\_MB\_DQS\_H0 >> MEM\_MB\_DQS\_H0 153  
(5) MEM\_MB\_DQS\_L0 >> MEM\_MB\_DQS\_L0 152  
(5) MEM\_MB\_CLK\_H2 >> MEM\_MB\_CLK\_H2 218  
(5) MEM\_MB\_CLK\_L2 >> MEM\_MB\_CLK\_L2 219  
(5) MEM\_MB\_CLK\_H0 >> MEM\_MB\_CLK\_H0 74  
(5) MEM\_MB\_CLK\_L0 >> MEM\_MB\_CLK\_L0 75  
(5) MEM\_MB\_C2 >> MEM\_MB\_C2 236  
(5) MEM\_MB\_CS\_L3 >> MEM\_MB\_CS\_L3 237  
(5) MEM\_MB\_CS\_L2 >> MEM\_MB\_CS\_L2 93  
(5) MEM\_MB\_CS\_L1 >> MEM\_MB\_CS\_L1 89  
(5) MEM\_MB\_CS\_L0 >> MEM\_MB\_CS\_L0 84  
(5) MEM\_MB\_CKE1 >> MEM\_MB\_CKE1 203  
(5) MEM\_MB\_CKE0 >> MEM\_MB\_CKE0 60  
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(5) MEM\_MB\_ODT0 >> MEM\_MB\_ODT0 87  
199 CB-7  
154 CB-6  
192 CB-5  
47 CB-4  
201 CB-3  
56 CB-2  
194 CB-1  
49 CB-0  
58 RESET\_N  
78 EVENT\_N  
208 ALERT\_N  
62 ACT\_N  
222 PAR  
230 SAVE\_N\_NC  
144 RFU-0  
205 RFU-1  
227 RFU-2

DDRIV-288P\_BLACK-RH-5

MEM\_MB\_DATA[63..0]

&gt;&gt;&gt; MEM\_MB\_DATA[63..0] (5)

DQ-63 280 MEM\_MB\_DATA63  
135 MEM\_MB\_DATA62  
DQ-62 273 MEM\_MB\_DATA61  
DQ-61 128 MEM\_MB\_DATA60  
DQ-60 282 MEM\_MB\_DATA59  
DQ-59 137 MEM\_MB\_DATA58  
DQ-58 275 MEM\_MB\_DATA57  
DQ-57 130 MEM\_MB\_DATA56  
DQ-56 269 MEM\_MB\_DATA55  
DQ-55 124 MEM\_MB\_DATA54  
DQ-54 262 MEM\_MB\_DATA53  
DQ-53 117 MEM\_MB\_DATA52  
DQ-52 271 MEM\_MB\_DATA51  
DQ-51 126 MEM\_MB\_DATA50  
DQ-50 264 MEM\_MB\_DATA49  
DQ-49 119 MEM\_MB\_DATA48  
DQ-48 258 MEM\_MB\_DATA47  
DQ-47 113 MEM\_MB\_DATA46  
DQ-46 251 MEM\_MB\_DATA45  
DQ-45 106 MEM\_MB\_DATA44  
DQ-44 260 MEM\_MB\_DATA43  
DQ-43 115 MEM\_MB\_DATA42  
DQ-42 253 MEM\_MB\_DATA41  
DQ-41 108 MEM\_MB\_DATA40  
DQ-40 247 MEM\_MB\_DATA39  
DQ-39 102 MEM\_MB\_DATA38  
DQ-38 240 MEM\_MB\_DATA37  
DQ-37 85 MEM\_MB\_DATA36  
DQ-36 249 MEM\_MB\_DATA35  
DQ-35 104 MEM\_MB\_DATA34  
DQ-34 242 MEM\_MB\_DATA33  
DQ-33 97 MEM\_MB\_DATA32  
DQ-32 188 MEM\_MB\_DATA31  
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DQ-30 181 MEM\_MB\_DATA29  
DQ-29 36 MEM\_MB\_DATA28  
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DQ-15 21 MEM\_MB\_DATA14  
DQ-14 159 MEM\_MB\_DATA13  
DQ-13 14 MEM\_MB\_DATA12  
DQ-12 168 MEM\_MB\_DATA11  
DQ-11 23 MEM\_MB\_DATA10  
DQ-10 161 MEM\_MB\_DATA9  
DQ-9 16 MEM\_MB\_DATA8  
DQ-8 155 MEM\_MB\_DATA7  
DQ-7 10 MEM\_MB\_DATA6  
DQ-6 148 MEM\_MB\_DATA5  
DQ-5 3 MEM\_MB\_DATA4  
DQ-4 157 MEM\_MB\_DATA3  
DQ-3 12 MEM\_MB\_DATA2  
DQ-2 150 MEM\_MB\_DATA1  
DQ-1 5 MEM\_MB\_DATA0  
207 MEM\_MB\_BG\_1 >> MEM\_MB\_BG\_1 (5)  
63 MEM\_MB\_BG\_0 >> MEM\_MB\_BG\_0 (5)  
224 MEM\_MB\_BA\_1 >> MEM\_MB\_BA\_1 (5)  
81 MEM\_MB\_BA\_0 >> MEM\_MB\_BA\_0 (5)  
234 MEM\_MB\_ADD17 >> MEM\_MB\_ADD17 (5)  
82 MEM\_MB\_ADD16 >> MEM\_MB\_ADD16 (5)  
86 MEM\_MB\_ADD15 >> MEM\_MB\_ADD15 (5)  
228 MEM\_MB\_ADD14 >> MEM\_MB\_ADD14 (5)  
232 MEM\_MB\_ADD13 >> MEM\_MB\_ADD13 (5)  
65 MEM\_MB\_ADD12 >> MEM\_MB\_ADD12 (5)  
210 MEM\_MB\_ADD11 >> MEM\_MB\_ADD11 (5)  
225 MEM\_MB\_ADD10 >> MEM\_MB\_ADD10 (5)  
66 MEM\_MB\_ADD9 >> MEM\_MB\_ADD9 (5)  
211 MEM\_MB\_ADD8 >> MEM\_MB\_ADD8 (5)  
66 MEM\_MB\_ADD7 >> MEM\_MB\_ADD7 (5)  
211 MEM\_MB\_ADD6 >> MEM\_MB\_ADD6 (5)  
69 MEM\_MB\_ADD5 >> MEM\_MB\_ADD5 (5)  
213 MEM\_MB\_ADD4 >> MEM\_MB\_ADD4 (5)  
214 MEM\_MB\_ADD3 >> MEM\_MB\_ADD3 (5)  
71 MEM\_MB\_ADD2 >> MEM\_MB\_ADD2 (5)  
72 MEM\_MB\_ADD1 >> MEM\_MB\_ADD1 (5)  
79 MEM\_MB\_ADD0 >> MEM\_MB\_ADD0 (5)  
A17  
A16\_RAS\_N  
A15\_CAS\_N  
A14\_WE\_N  
A13  
A12  
A11  
A10  
A9  
A8  
A7  
A6  
A5  
A4  
A3  
A2  
A1  
A0  
141 DDR\_SCL\_C01 >> DDR\_SCL\_C01 (11)  
285 DDR\_SDA\_C01 >> DDR\_SDA\_C01 (11)  
238 +VPP25\_SPD\_C01  
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139

DIMM3 (CHANNEL-B0)

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DIMM3 CH1 ADDRESS HEX:4

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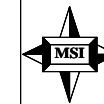
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99 DQS13P  
100 DQS13N  
40 DQS12P  
41 DQS12N  
29 DQS11P  
30 DQS11N  
18 DQS10P  
19 DQS10N  
7 DQS9P  
8 DQS9N  
197 DQS8P  
196 DQS8N  
(5) MEM\_MB\_DQS\_H7 >> MEM\_MB\_DQS\_H7 278  
(5) MEM\_MB\_DQS\_L7 >> MEM\_MB\_DQS\_L7 277  
(5) MEM\_MB\_DQS\_H6 >> MEM\_MB\_DQS\_H6 267  
(5) MEM\_MB\_DQS\_L6 >> MEM\_MB\_DQS\_L6 266  
(5) MEM\_MB\_DQS\_H5 >> MEM\_MB\_DQS\_H5 256  
(5) MEM\_MB\_DQS\_L5 >> MEM\_MB\_DQS\_L5 255  
(5) MEM\_MB\_DQS\_H4 >> MEM\_MB\_DQS\_H4 245  
(5) MEM\_MB\_DQS\_L4 >> MEM\_MB\_DQS\_L4 244  
(5) MEM\_MB\_DQS\_H3 >> MEM\_MB\_DQS\_H3 186  
(5) MEM\_MB\_DQS\_L3 >> MEM\_MB\_DQS\_L3 185  
(5) MEM\_MB\_DQS\_H2 >> MEM\_MB\_DQS\_H2 175  
(5) MEM\_MB\_DQS\_L2 >> MEM\_MB\_DQS\_L2 174  
(5) MEM\_MB\_DQS\_H1 >> MEM\_MB\_DQS\_H1 164  
(5) MEM\_MB\_DQS\_L1 >> MEM\_MB\_DQS\_L1 163  
(5) MEM\_MB\_DQS\_H0 >> MEM\_MB\_DQS\_H0 153  
(5) MEM\_MB\_DQS\_L0 >> MEM\_MB\_DQS\_L0 152  
(5) MEM\_MB\_CLK\_H3 >> MEM\_MB\_CLK\_H3 218  
(5) MEM\_MB\_CLK\_L3 >> MEM\_MB\_CLK\_L3 219  
(5) MEM\_MB\_CLK\_H1 >> MEM\_MB\_CLK\_H1 74  
(5) MEM\_MB\_CLK\_L1 >> MEM\_MB\_CLK\_L1 75  
(5) MEM\_MB\_C2 >> MEM\_MB\_C2 236  
(5) MEM\_MB\_CS\_L7 >> MEM\_MB\_CS\_L7 237  
(5) MEM\_MB\_CS\_L6 >> MEM\_MB\_CS\_L6 93  
(5) MEM\_MB\_CS\_L5 >> MEM\_MB\_CS\_L5 89  
(5) MEM\_MB\_CS\_L4 >> MEM\_MB\_CS\_L4 84  
(5) MEM\_MB\_CKE3 >> MEM\_MB\_CKE3 203  
(5) MEM\_MB\_CKE2 >> MEM\_MB\_CKE2 60  
(5) MEM\_MB\_ODT3 >> MEM\_MB\_ODT3 91  
(5) MEM\_MB\_ODT2 >> MEM\_MB\_ODT2 87  
199 CB-7  
154 CB-6  
192 CB-5  
47 CB-4  
201 CB-3  
56 CB-2  
194 CB-1  
49 CB-0  
58 RESET\_N  
78 EVENT\_N  
208 ALERT\_N  
62 ACT\_N  
222 PAR  
230 SAVE\_N\_NC  
144 RFU-0  
140 RFU-1  
205 RFU-2  
227

DIMM4 (CHANNEL-B1)

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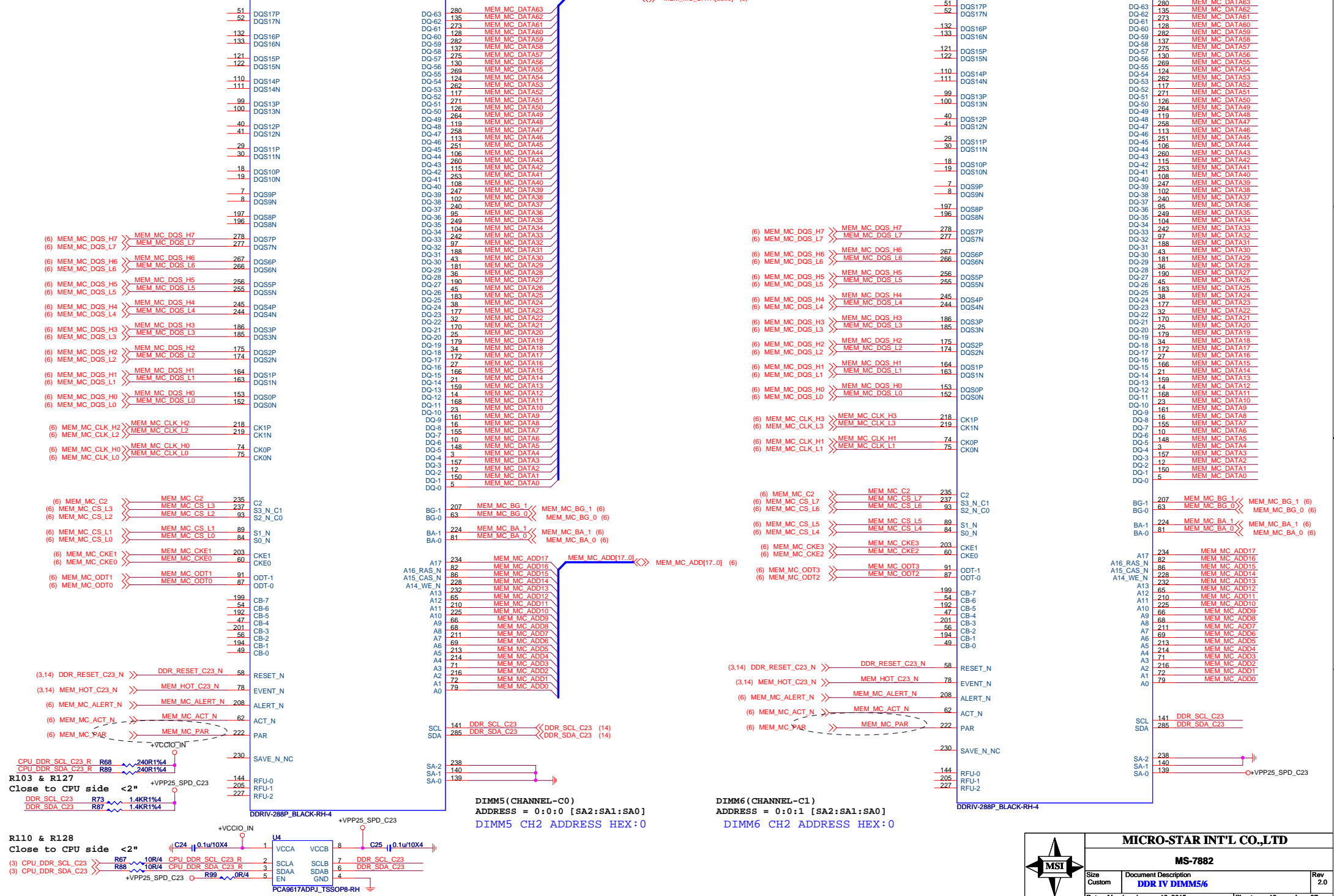


MICRO-STAR INT'L CO.,LTD

MS-7882

Size	Document Description	Rev
Custom	DDR IV DIMM3/4	2.0
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## DDR IV DIMM5/6

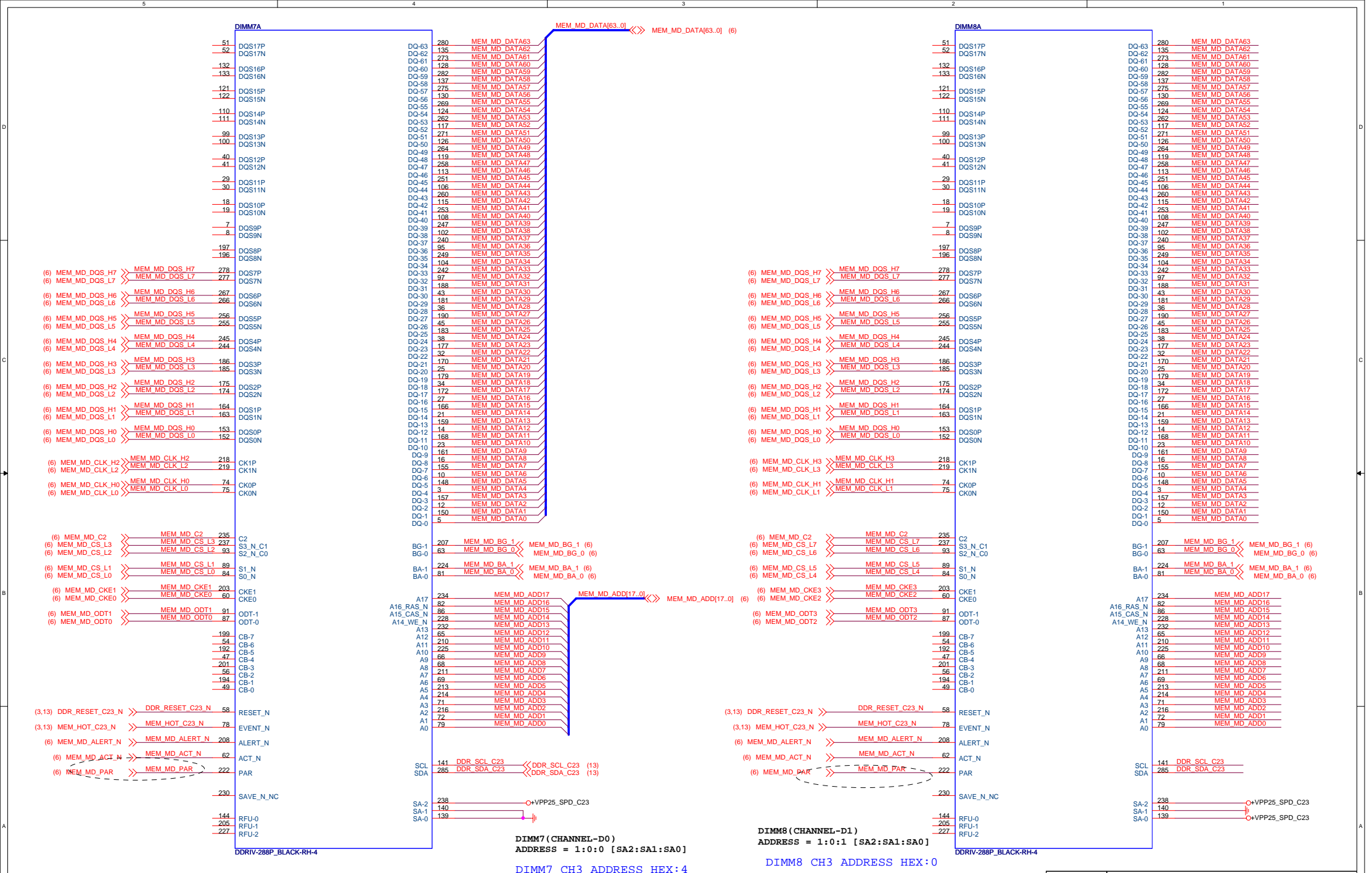


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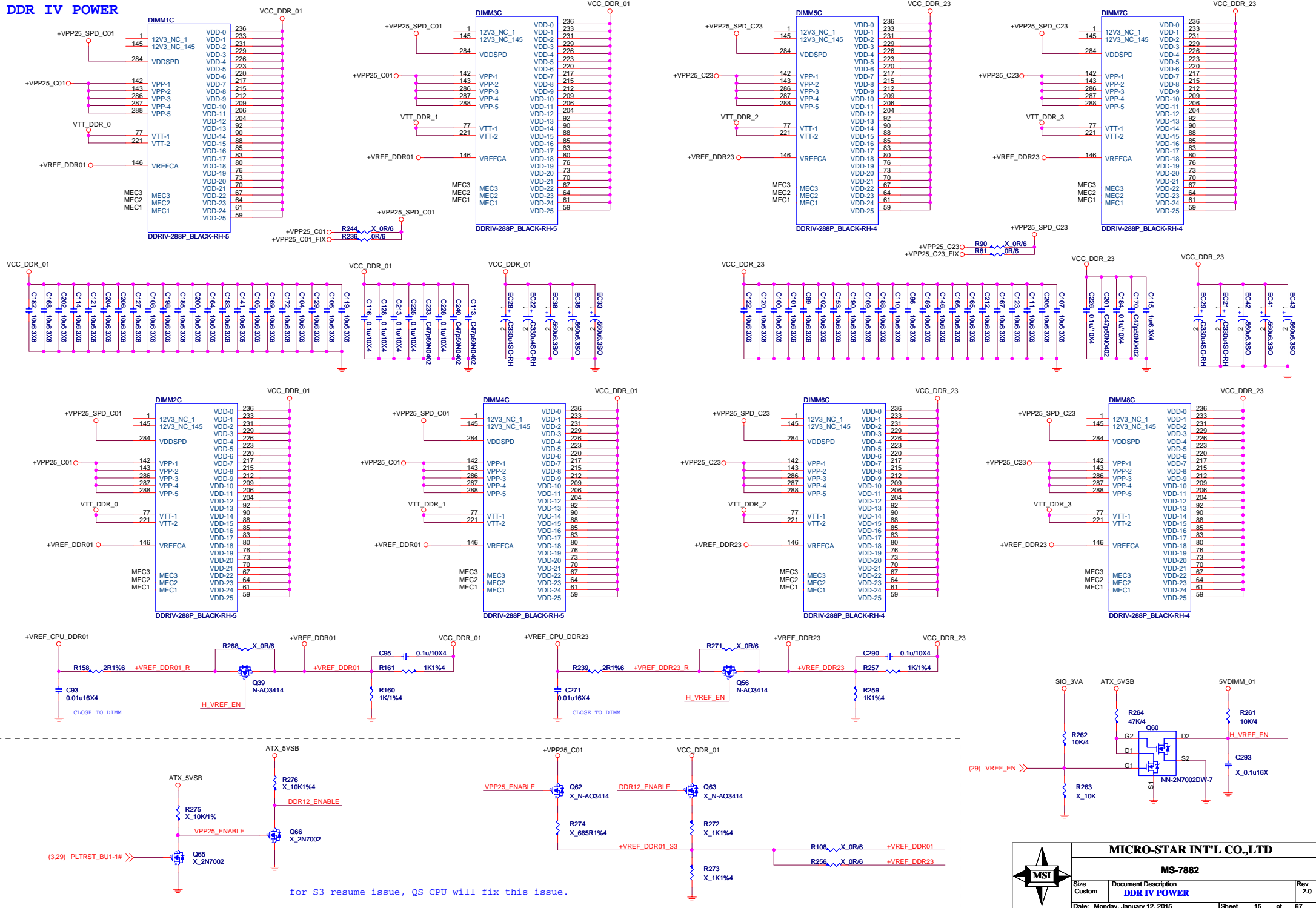
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Date: Monday, January 12, 2015		Sheet 13 of 67





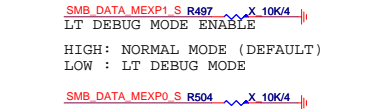
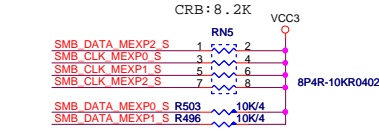
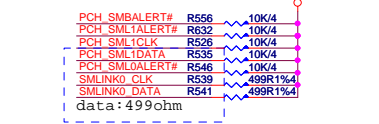
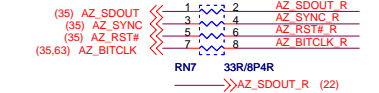


# DDR IV POWER



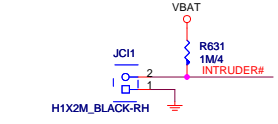


PCH-LPC/HDA/RTC/MISC/SPI

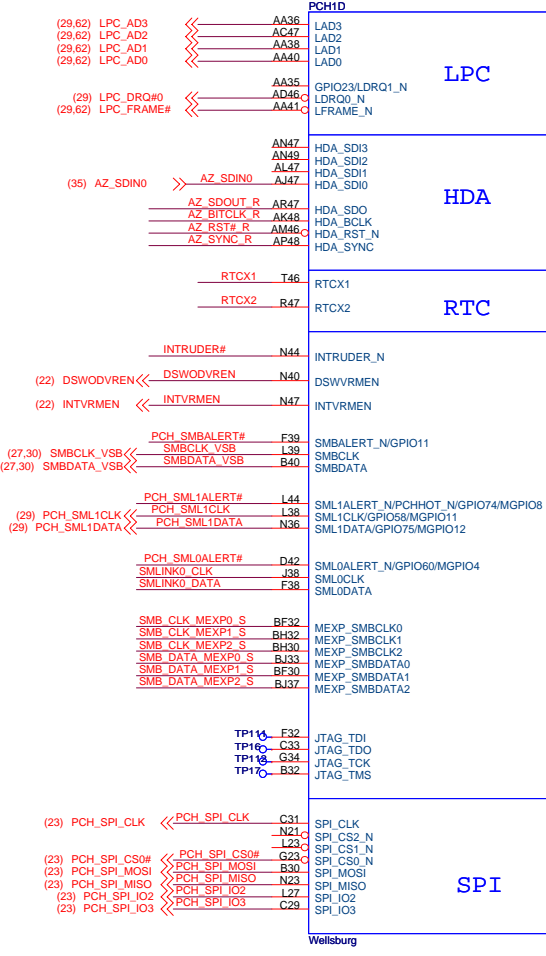
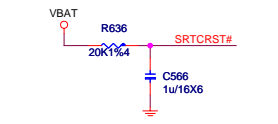
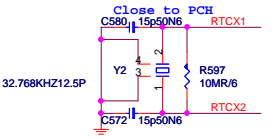


ADR TIMER HOLD OFF (DEFENSIVE)  
NOTE: EXT PU ON SMB  
HIGH: NORMAL MODE (DEFAULT)  
LOW : ADR TIMER HOLD OFF

Chassis Intrusion

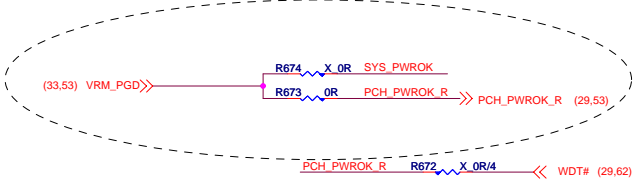


RTC Block

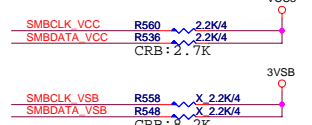
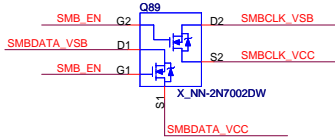
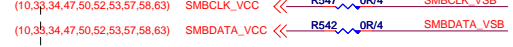
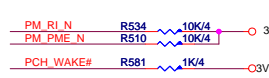
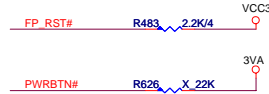
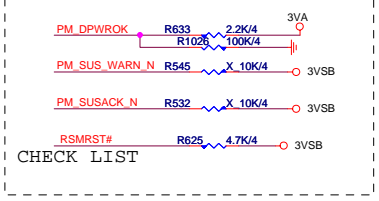
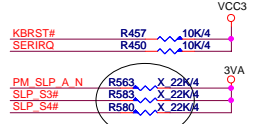
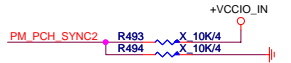
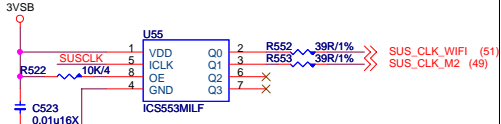
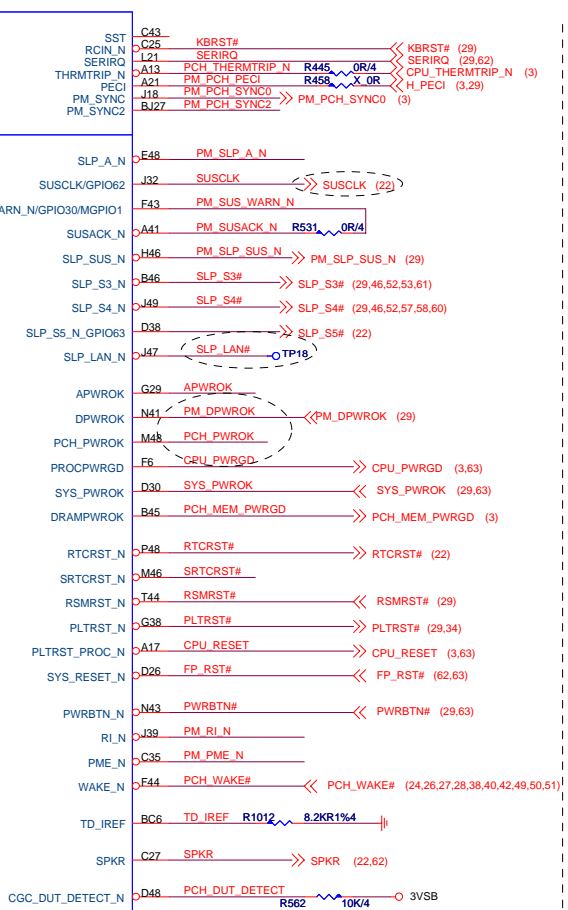
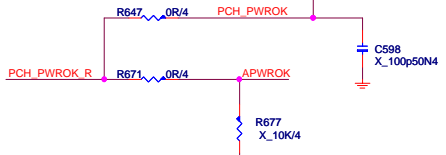


power management

The negative min timing implies that DRAMPWROK must either fall before SLP\_S4# or within 100 ns after it.



Trace length of APWROK must be less than PCH\_PWROK

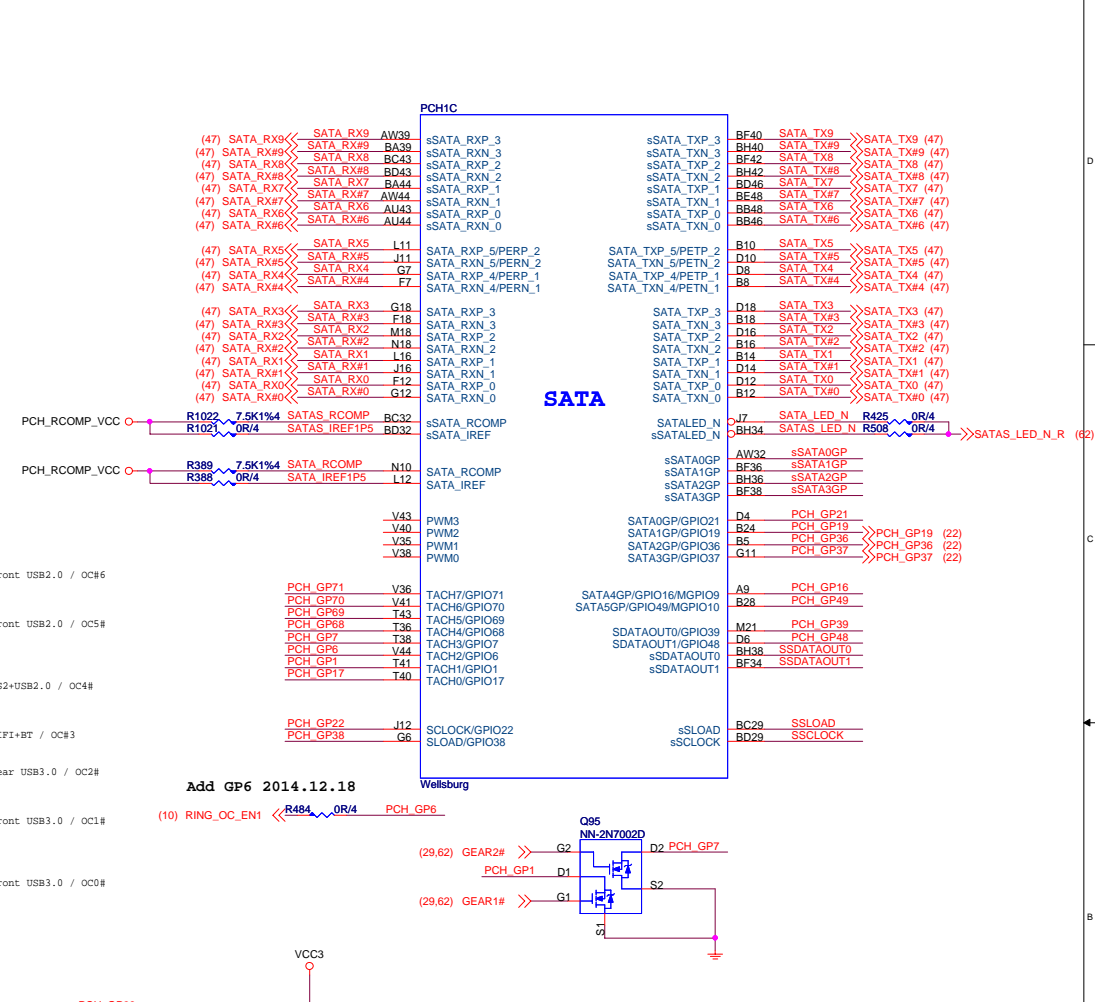
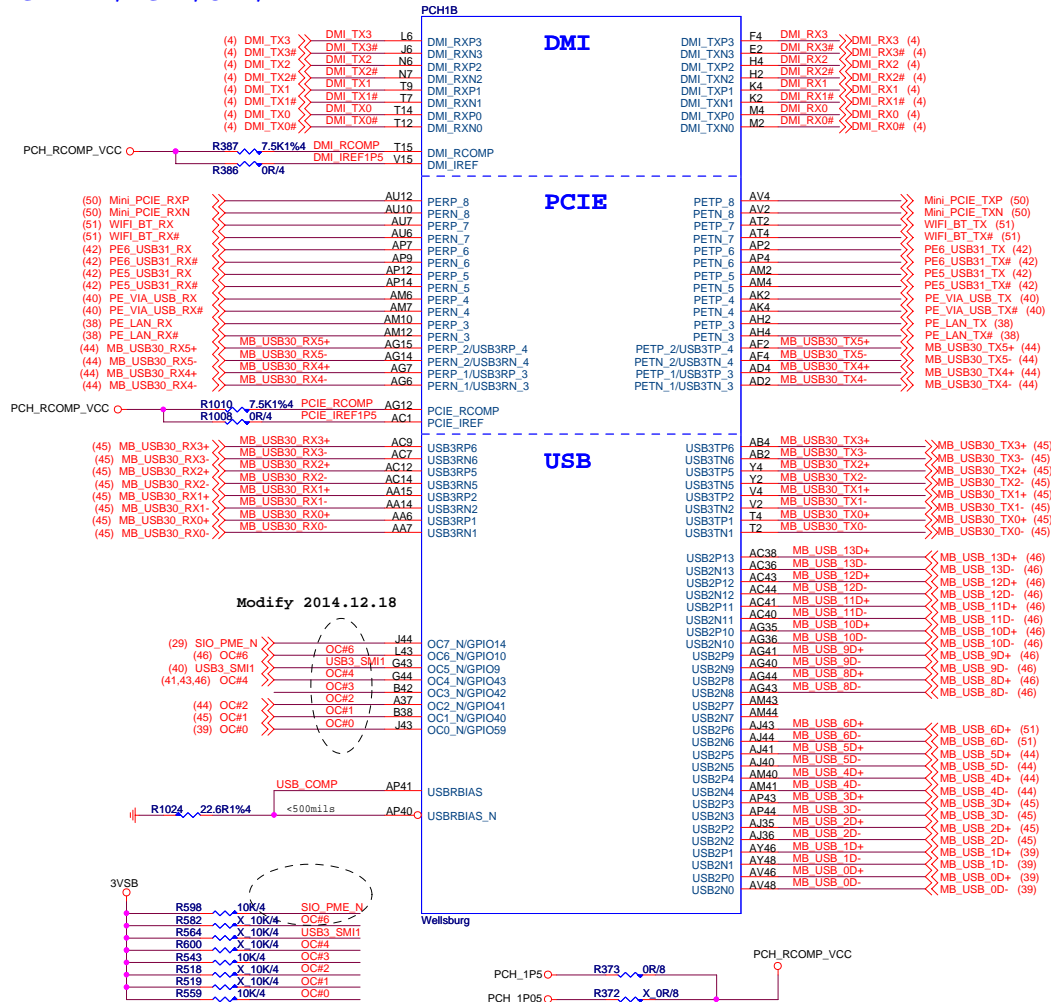


MICRO-STAR INT'L CO.,LTD

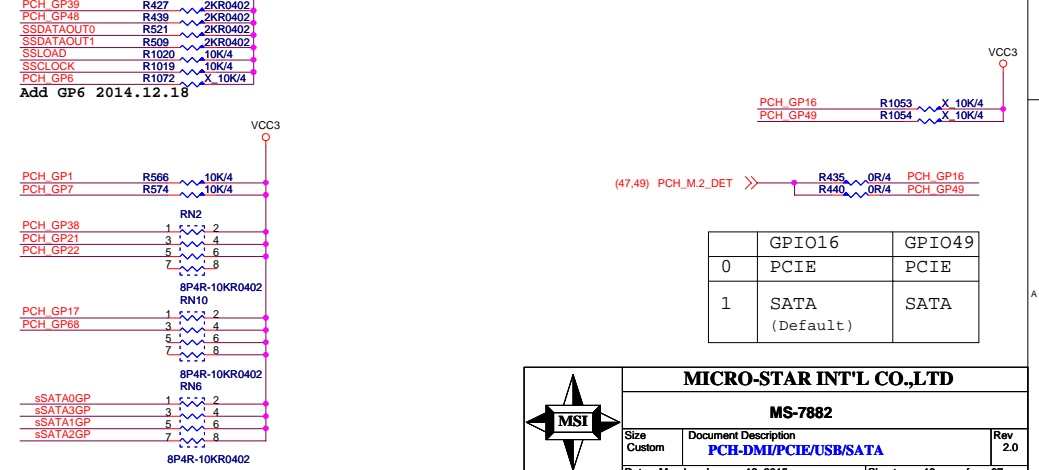
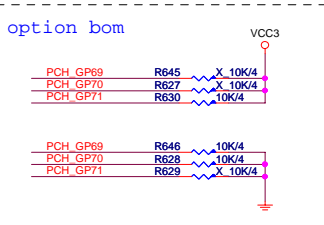
MS-7882

Size Custom	Document Description PCH-LPC/HDA/RTC/MISC/SPI	Rev 2.0
Date: Monday, January 12, 2015	Sheet 17	of 67

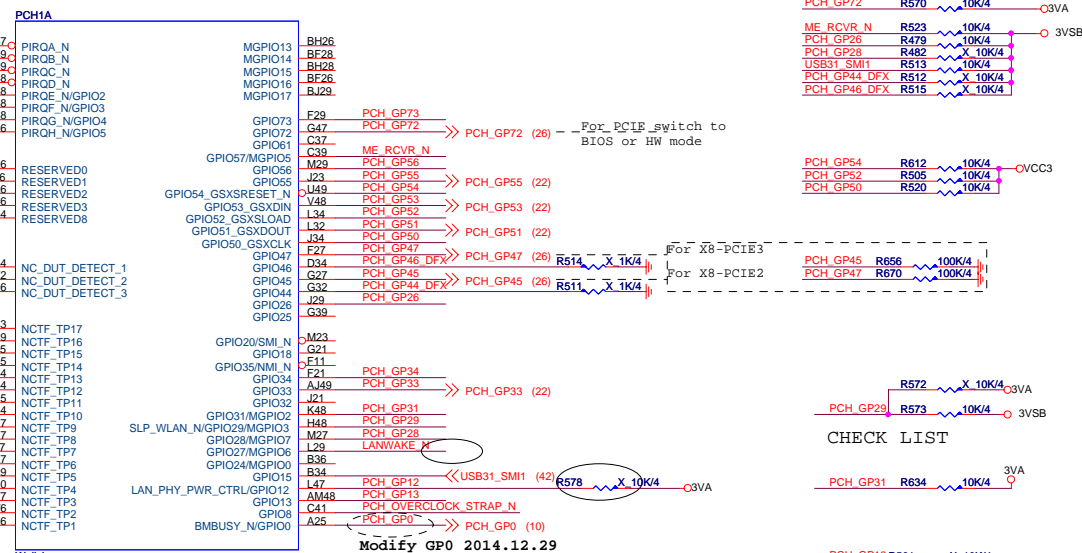
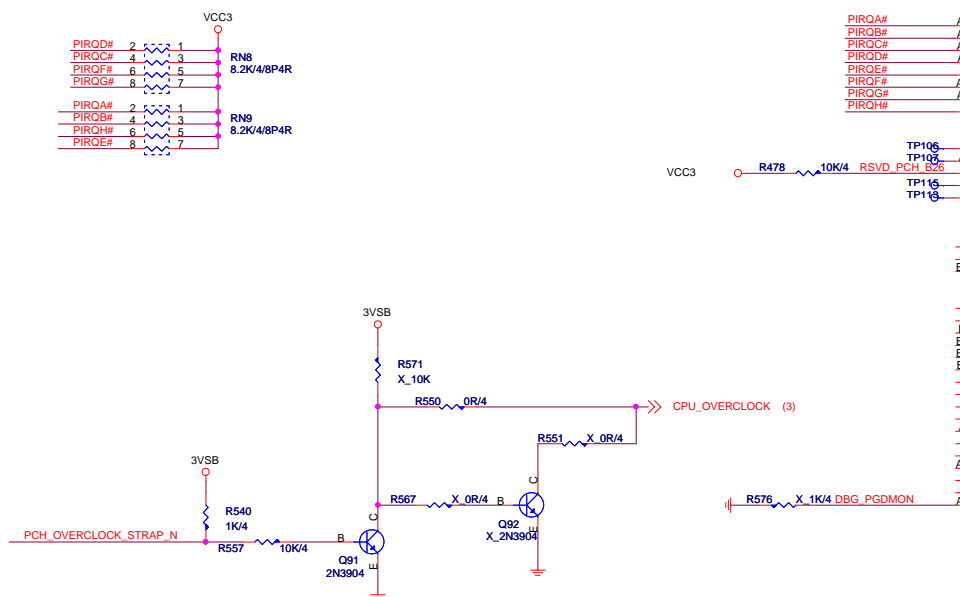
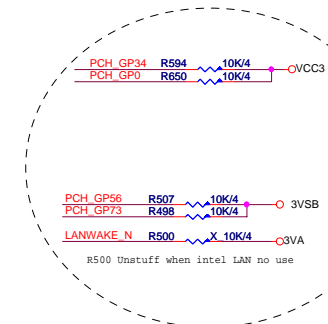
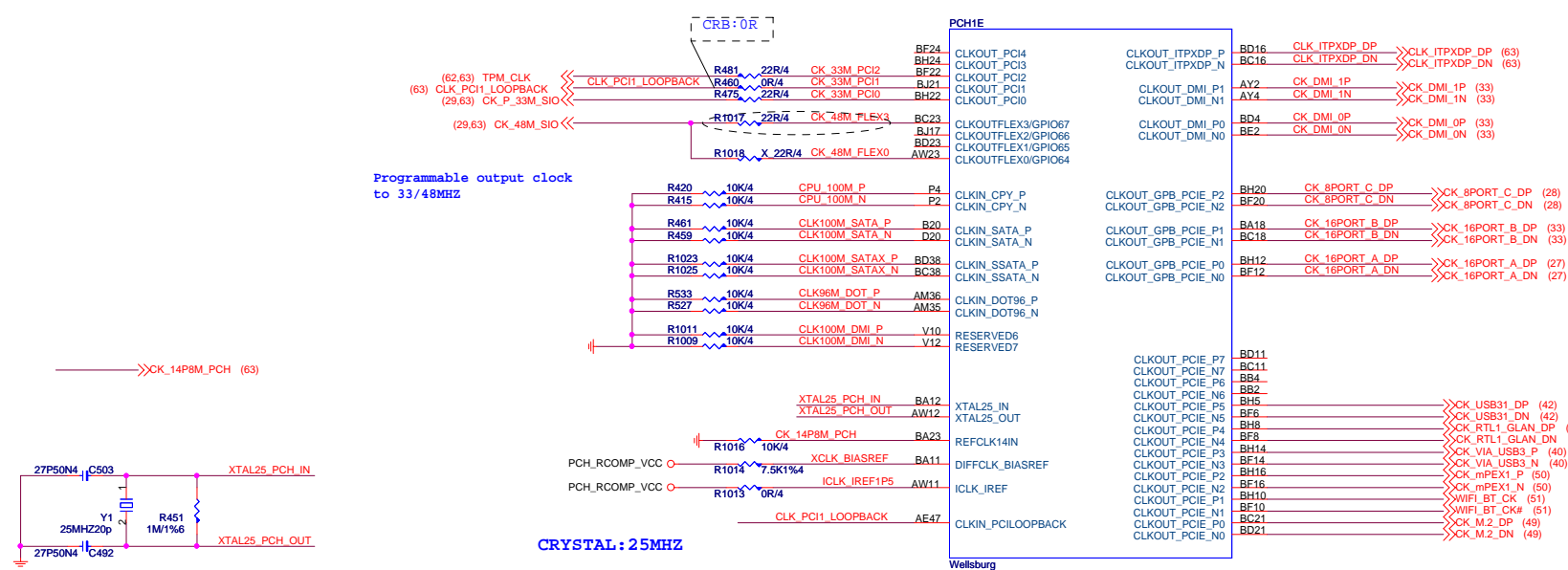
## PCH-DMI/PCIE/USB/SATA



GPIO	71	70	69
Default	1	1	1
ACK	1	1	0
U3.1	1	0	1
2.0	1	0	0



## PCH-CLK/GPIO



INTEGRATED CLOCK ENABLE

PCH\_OVERCLOCK\_STRAP\_N R544 2.2K/4

HIGH: DISABLE  
LOW : ENABLE



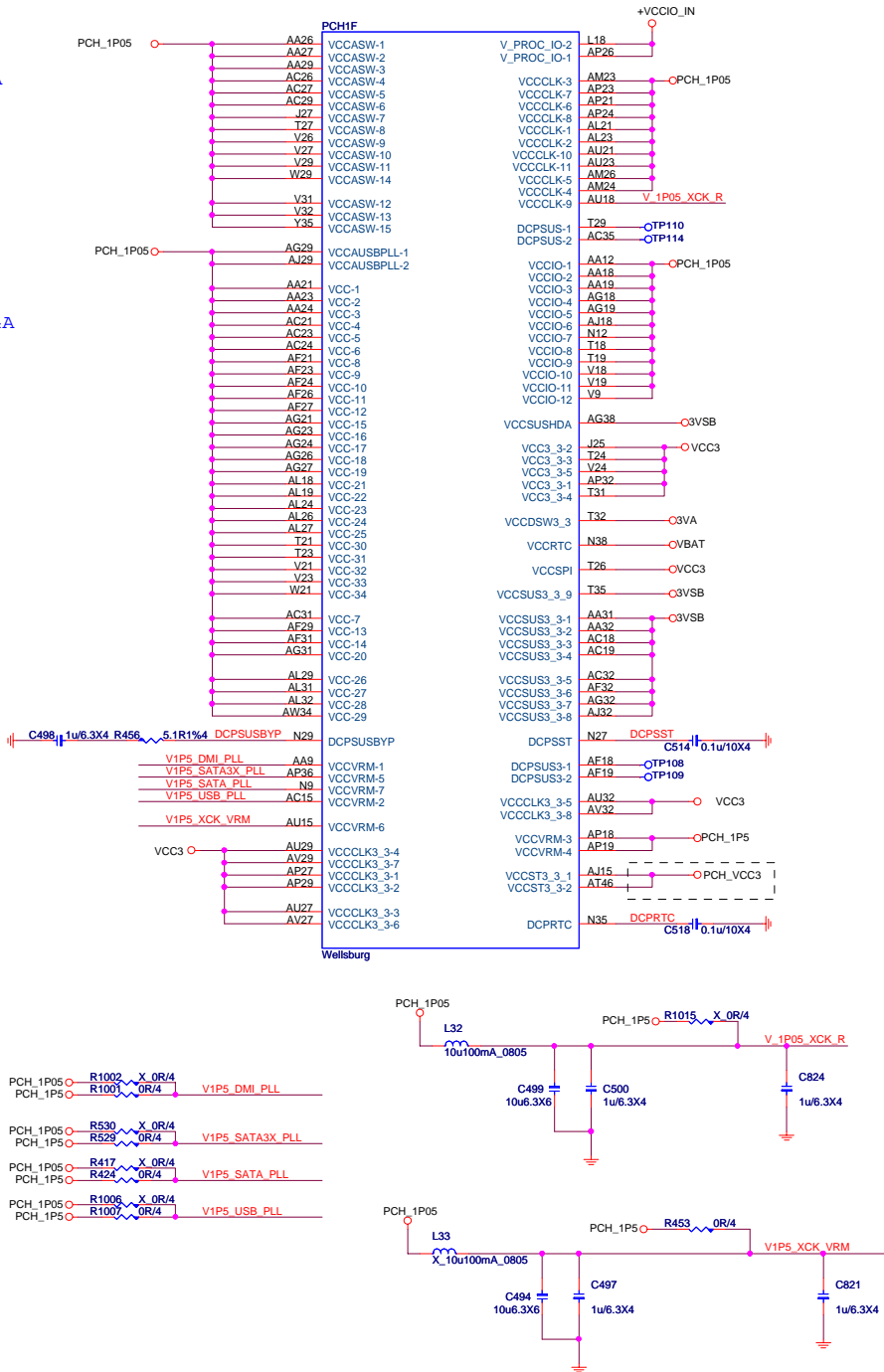
**MICRO-STAR INT'L CO.,LTD**

MS-7882

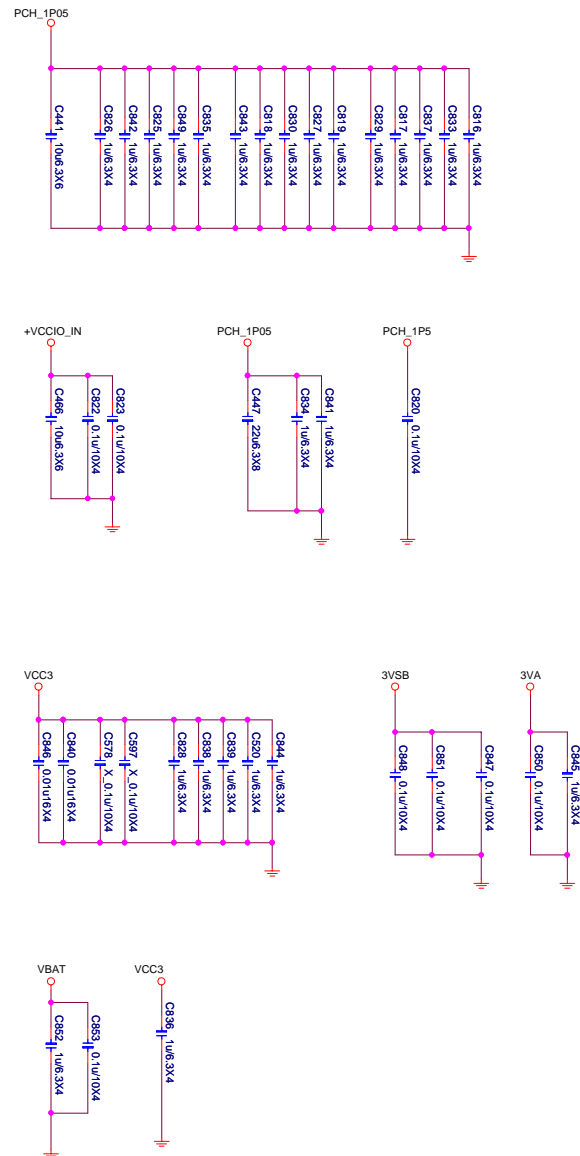
Size Custom	Document Description <b>PCH-CLK/GPIO</b>	Rev 2.0
Date: Monday, January 12, 2015		Sheet 19 of 67

PCH-POWER

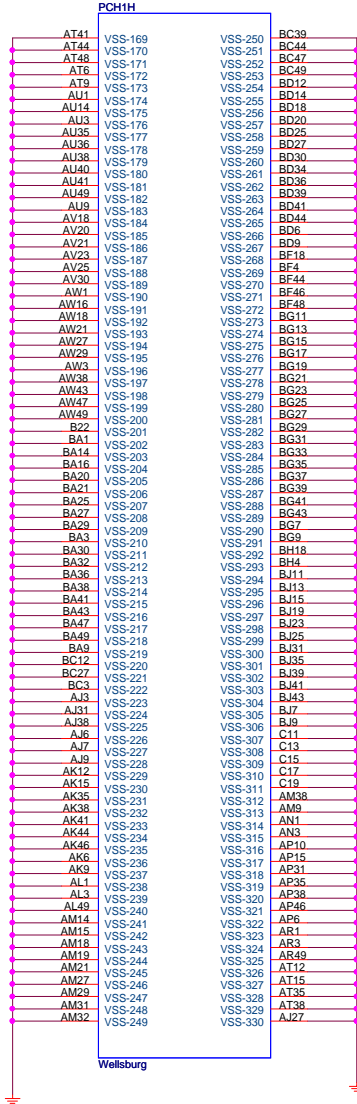
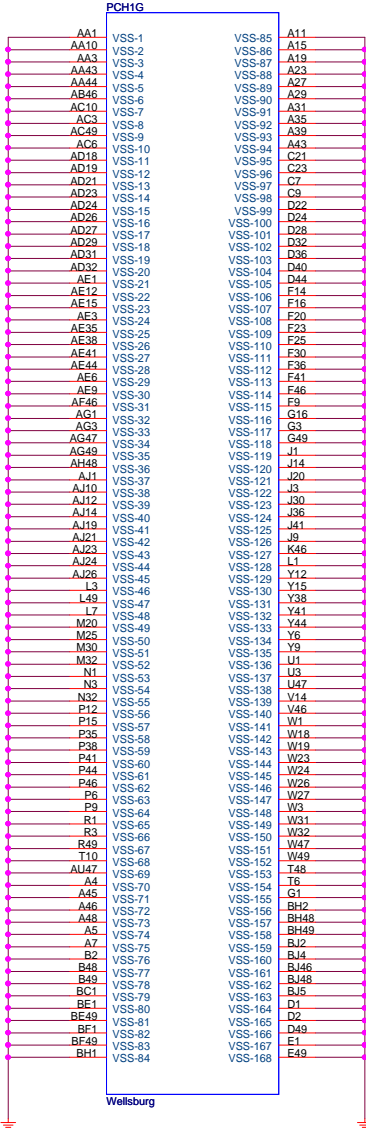
PCH\_1P05:5.83A  
+1P05V\_ME:0.67A  
VCC3:0.2A  
3VSB:0.27A  
SPI\_VCC3:0.02A  
3VA:0.02A  
+VCCIO\_IN:0.004A



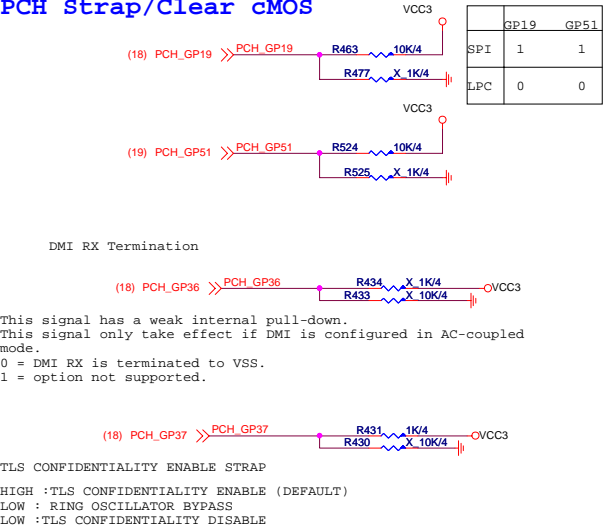
PCH decoupling cap



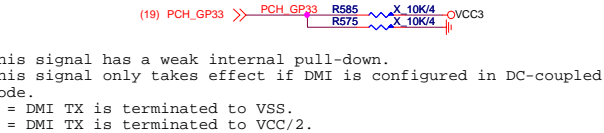




PCH Strap/Clear cMOS



DMI TX TERMINATION (DEFENSIVE)



HIGH (1-2):SECURITY MEASURES OVERRIDEN  
LOW (0-1) : SECURITY PER FLASH DESCRIPTOR (DEFAULT)

DEEP SLEEP WELL ON-DIE VRM ENABLE



HIGH: ENABLE (INTERNAL SUPPLY) (DEFAULT)  
LOW: DISABLE (EXTERNAL SUPPLY)

LOW : REBOOT  
HIGH: NO-REBOOT

NO REBOOT OPTION STRAP

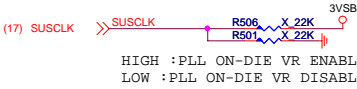


INTEGRATED SUS 1.05V VRM ENABLE

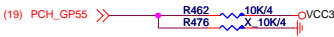


HIGH: ENABLE (INTERNAL SUPPLY) (DEFAULT)  
LOW: DISABLE (EXTERNAL SUPPLY)

PLL ON-DIE VR ENABLE



Top-Block Swap  
Override



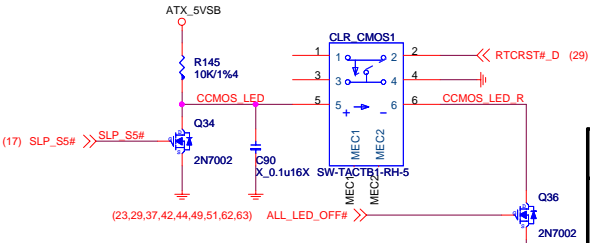
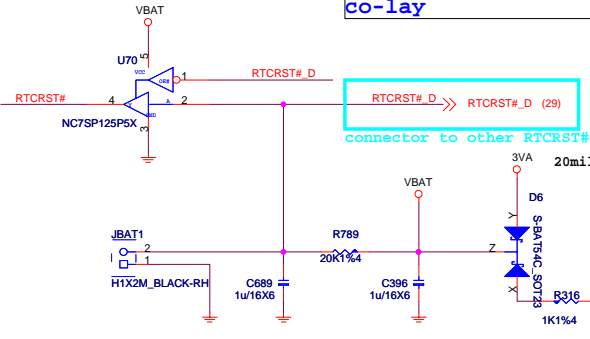
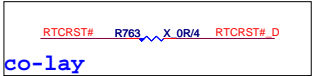
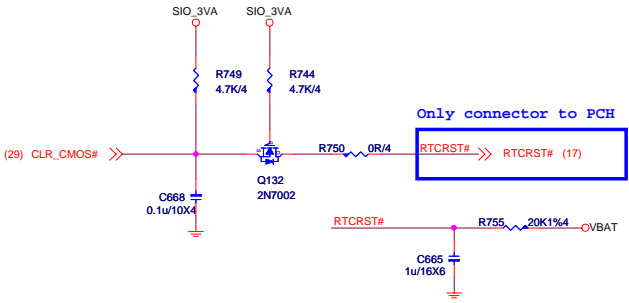
DMI AC Coupling

CHECK LIST



This Signal has a weak internal pull-up.  
0= Configures DMI for AC coupling mode.  
1 = Configures DMI for DC coupling mode.

RTC and CLR\_CMOS



LED LIGHTING RULE	
S0/S3/S4	: LED OFF
S5	: LED ON

tri-state		
INPUT		outout pin4
PIN1	PIN2	
L	H	H
L	L	L
H	X	Z

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**MS-7882**

Size Custom	Document Description PCH Strap/Clear cMOS	Rev 2.0
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(17) PCH\_SPI\_CS0# << PCH\_SPI\_CS0#

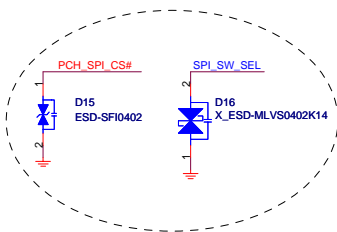
(17) PCH\_SPI\_MOSI << PCH\_SPI\_MOSI

(17) PCH\_SPI\_MISO << PCH\_SPI\_MISO

(17) PCH\_SPI\_CLK << PCH\_SPI\_CLK

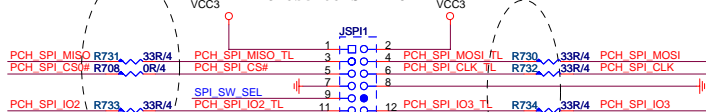
(17) PCH\_SPI\_IO2 << PCH\_SPI\_IO2

(17) PCH\_SPI\_IO3 << PCH\_SPI\_IO3



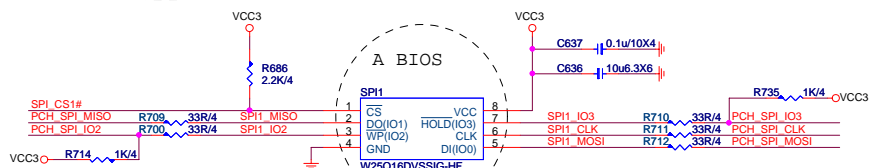
### SPI DEBUG PROT

Close to SPI ROM

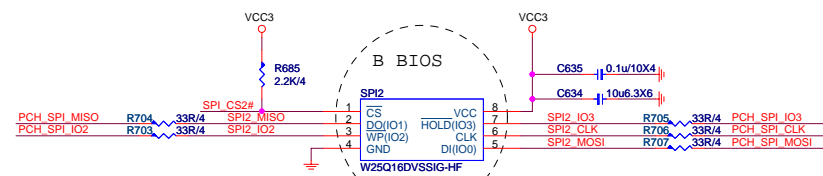


Part Number: N31-2061341-H06

(17) PCH\_PWROK >> PCH\_PWROK R1066 0R/4 SPI\_SW\_SEL 2014.06.05 Add for support TL624-1.1



16M ROM



### SPI FLASH ROM

Place close to SB.

\*SPI\_CLK & SPI\_MOSI must be length matched to within 500mils.  
\*SPI\_CLK & SPI\_CS# must be length matched to within 500mils.

(22,29,37,42,44,49,51,62,63) ALL\_LED\_OFF# >>

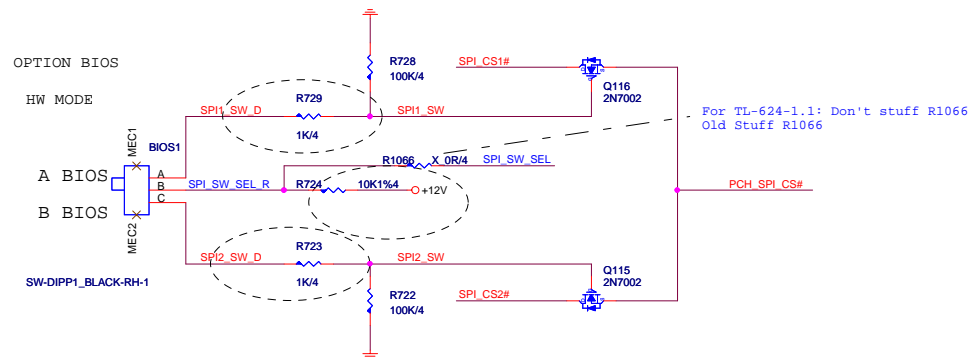
OPTION BIOS

HW MODE

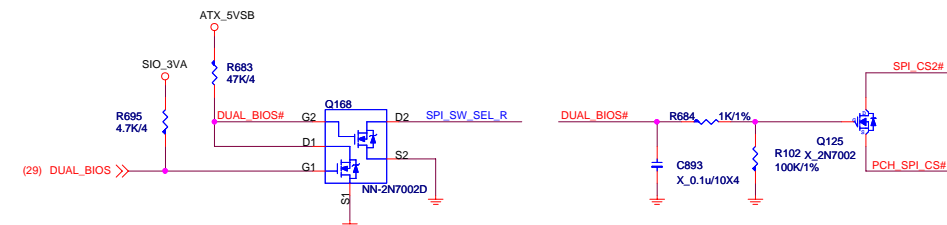
A BIOS

B BIOS

SW-DIPP1\_BLACK-RH-1



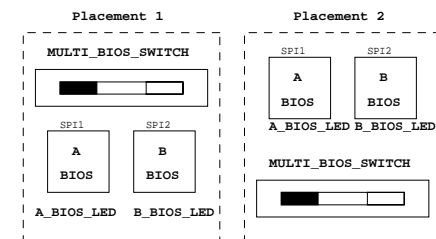
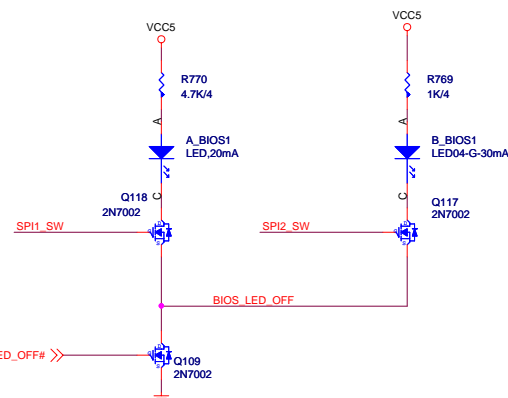
For auto testing in factory. Modify 2014.12.18



\* if you not support Standby power in S5 Status, component "MULTI\_BIOS\_SWITCH1.B(PIN B)" Pull-high to +12V & Q12/Q13 MOS select 2N7002

\* if you support Standby power in S5 Status(Ex: PCH is B75 Chipset), component "MULTI\_BIOS\_SWITCH1.B(PIN B)" pull-igh to ATX\_5VSB, component Q12/Q13 must select "Vth" under 1V (Component Suggestion as below)

D03-0341409-A68 / D03-0230019-A30



# PCIE1(X16) & PCIE2(X1) slots

(26,27,28) SMBCLK\_VSB\_R  
(26,27,28) SMBDATA\_VSB\_R

SMBCLK\_VSB\_R  
SMBDATA\_VSB\_R

VCC3  
3VSB

(17,26,27,28,38,40,42,49,50,51) PCH\_WAKE#

(4) EXP\_B\_TXP\_15  
(4) EXP\_B\_TXN\_15

(4) EXP\_B\_TXP\_14  
(4) EXP\_B\_TXN\_14

(4) EXP\_B\_TXP\_13  
(4) EXP\_B\_TXN\_13

(4) EXP\_B\_TXP\_12  
(4) EXP\_B\_TXN\_12

(4) EXP\_B\_TXP\_11  
(4) EXP\_B\_TXN\_11

(4) EXP\_B\_TXP\_10  
(4) EXP\_B\_TXN\_10

(4) EXP\_B\_TXP\_9  
(4) EXP\_B\_TXN\_9

(4) EXP\_B\_TXP\_8  
(4) EXP\_B\_TXN\_8

(25) PE1\_X16\_TXP7  
(25) PE1\_X16\_TXN7

(25) PE1\_X16\_TXP6  
(25) PE1\_X16\_TXN6

(25) PE1\_X16\_TXP5  
(25) PE1\_X16\_TXN5

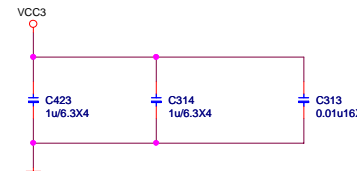
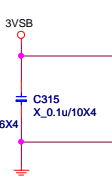
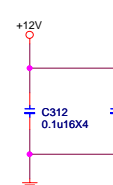
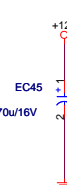
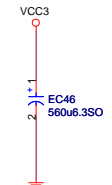
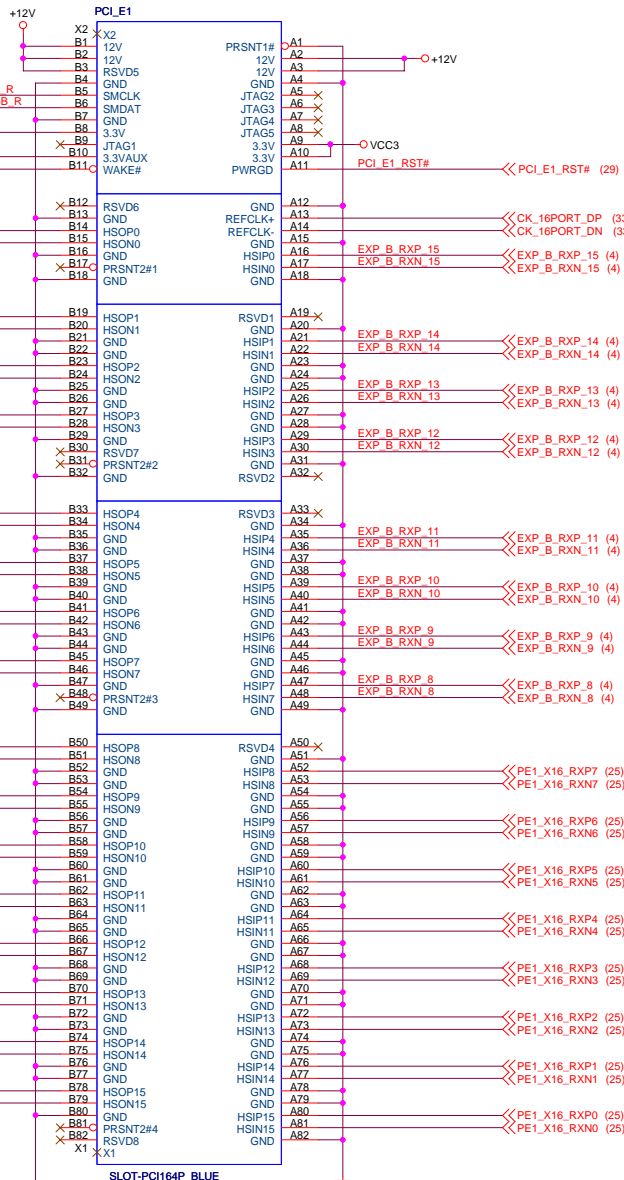
(25) PE1\_X16\_TXP4  
(25) PE1\_X16\_TXN4

(25) PE1\_X16\_TXP3  
(25) PE1\_X16\_TXN3

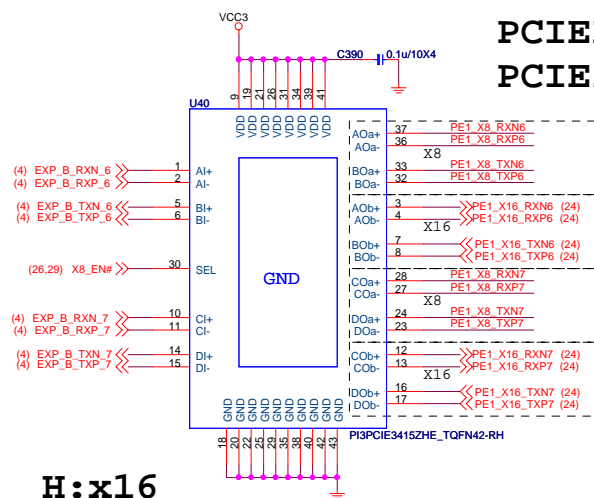
(25) PE1\_X16\_TXP2  
(25) PE1\_X16\_TXN2

(25) PE1\_X16\_TXP1  
(25) PE1\_X16\_TXN1

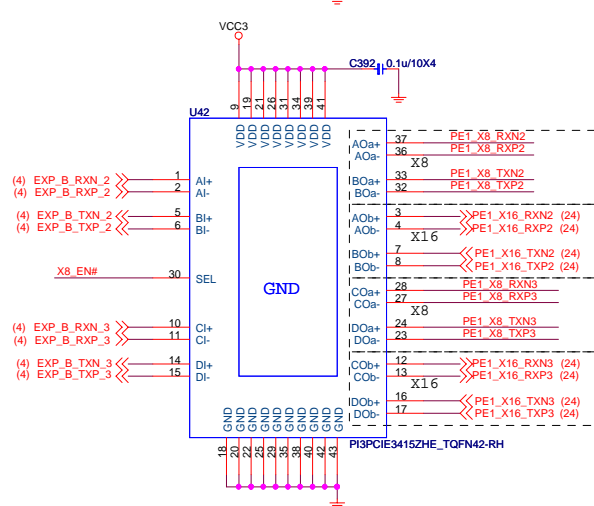
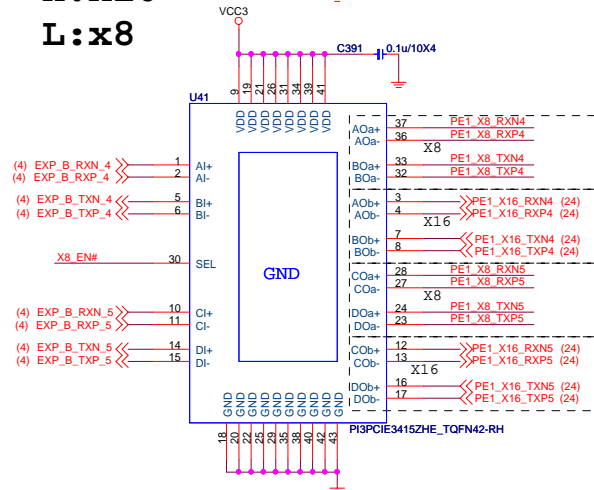
(25) PE1\_X16\_TXP0  
(25) PE1\_X16\_TXN0



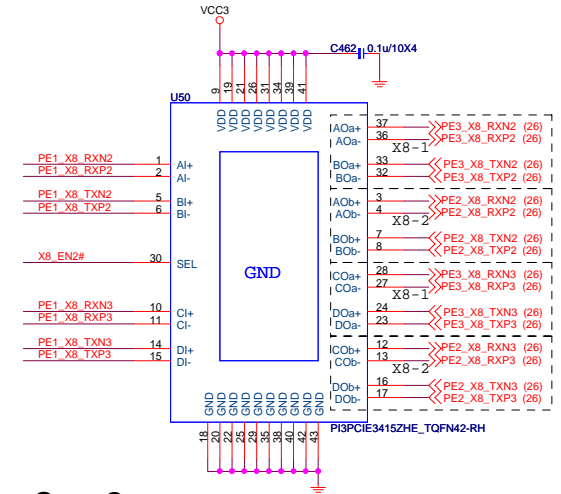
# PCIE1(x16) share to PCIE2(x8)



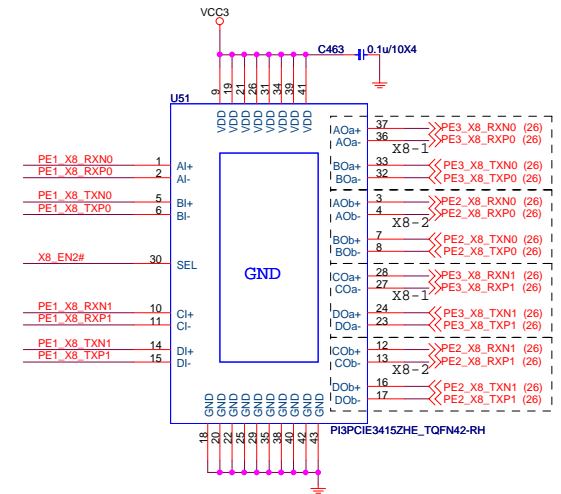
H:x16  
L:x8



# Switch PCIE(x8) for PCIE2 or PCIE3



H:x8-E2  
L:x8-E3



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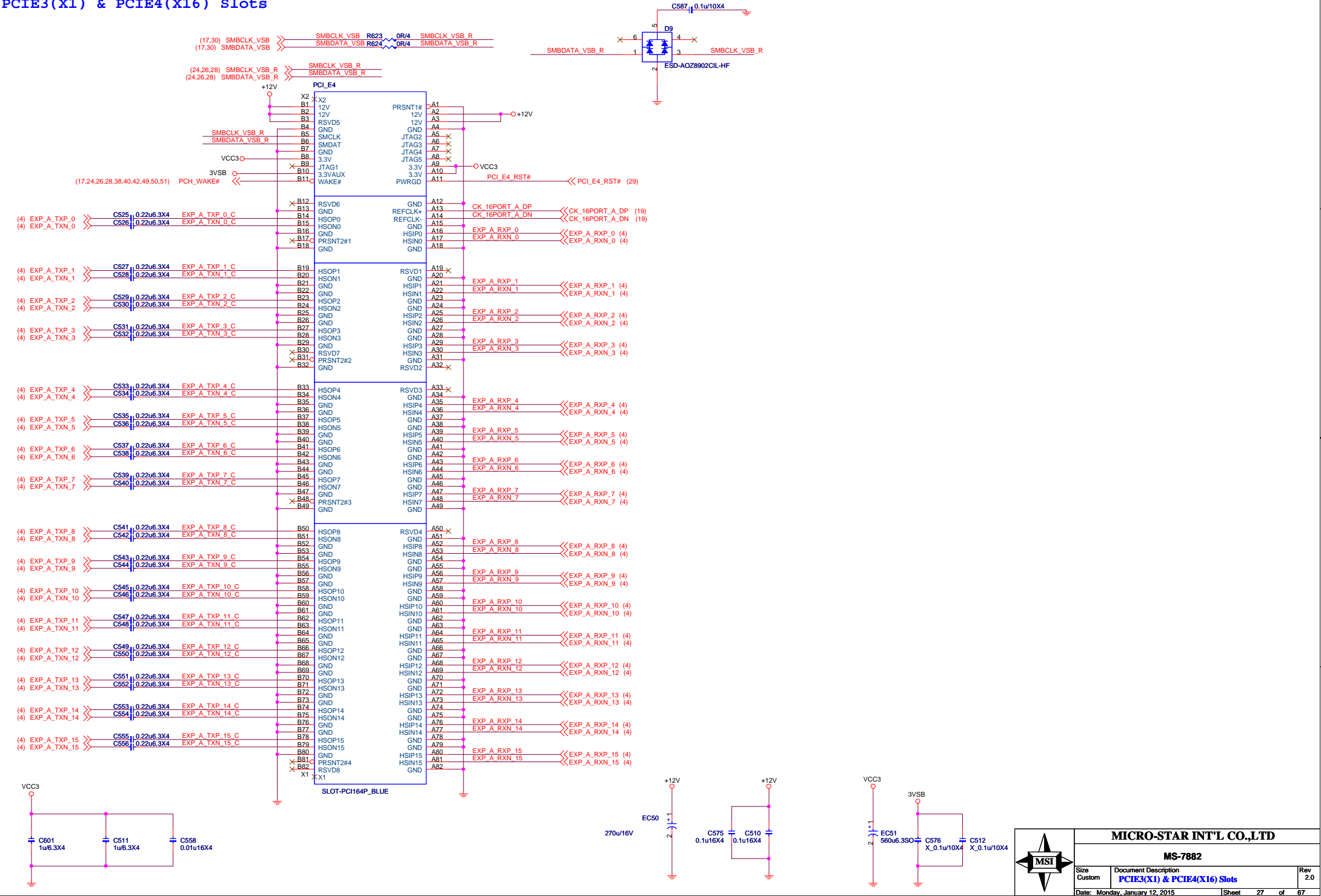
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Size	Document Description	Rev
Custom	PCIE Switch 3415	2.0
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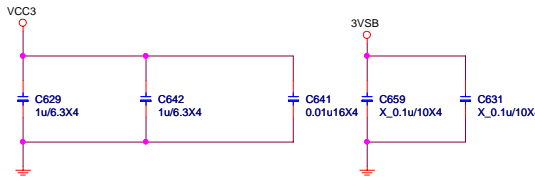
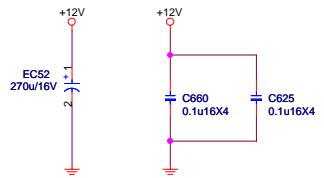
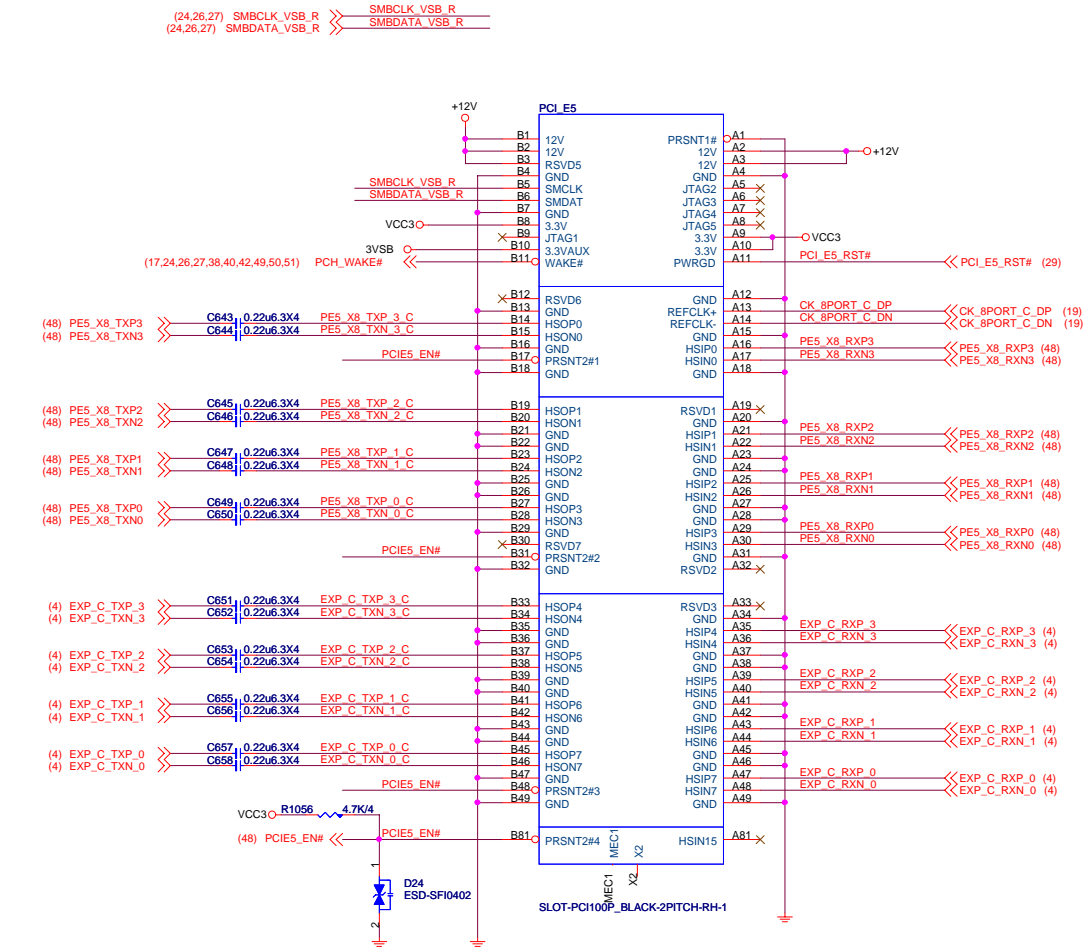




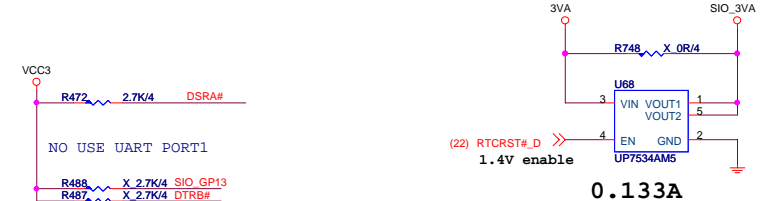
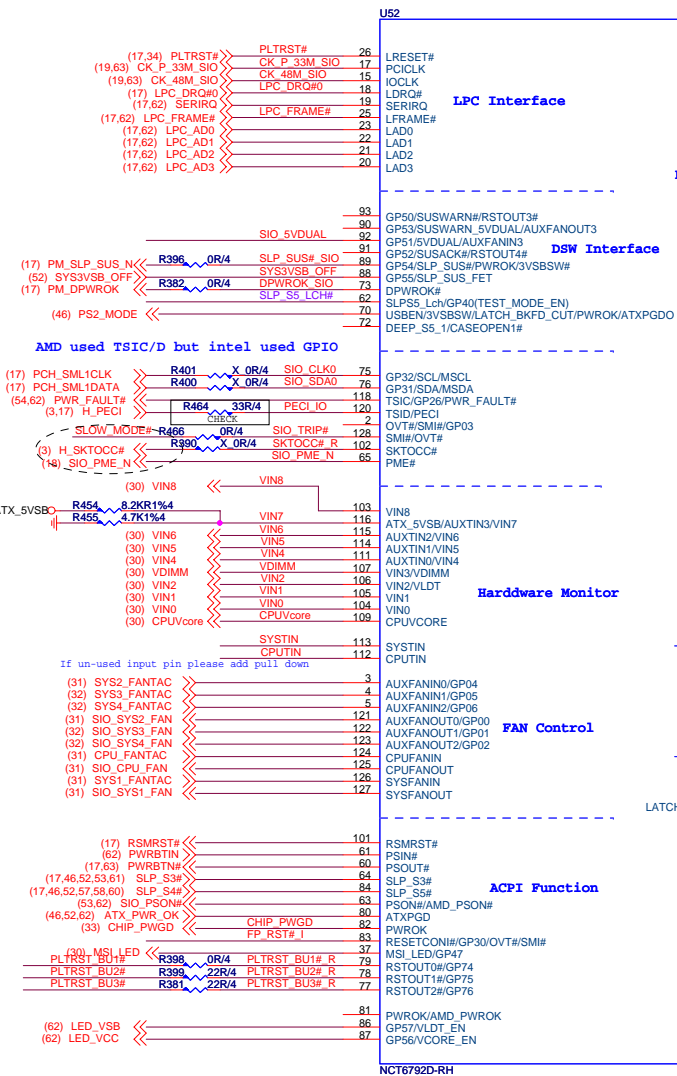
PCIE3(X1) & PCIE4(X16) Slots



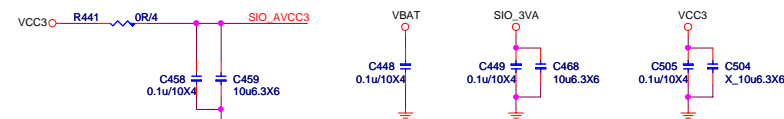
PCIE5(X8) Slots



## SIO-NTC6792D/PS2



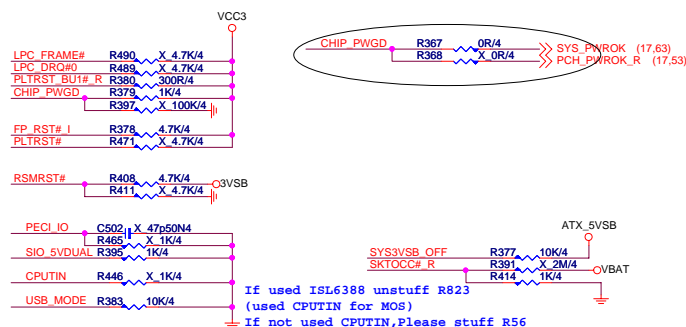
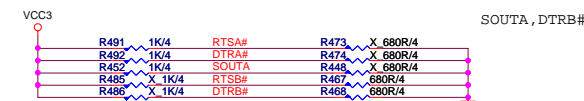
### 3V Analog Power



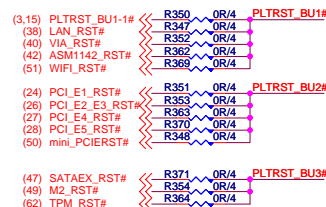
## POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

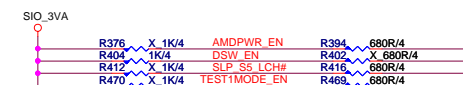
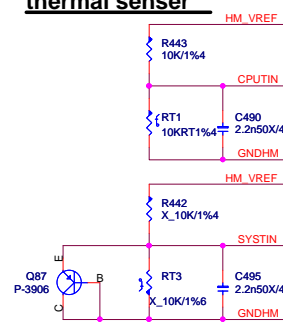
Note:  
If PIN34 strapping low, BIOS must programming LPT or GPIO



### PLTRST Damping R



thermal senser



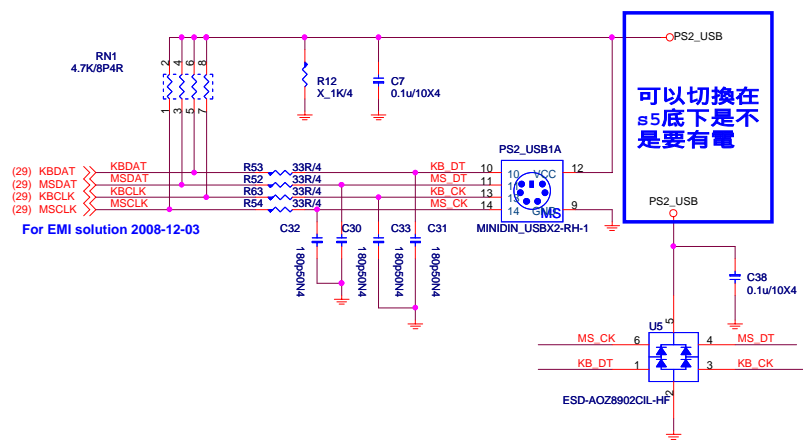
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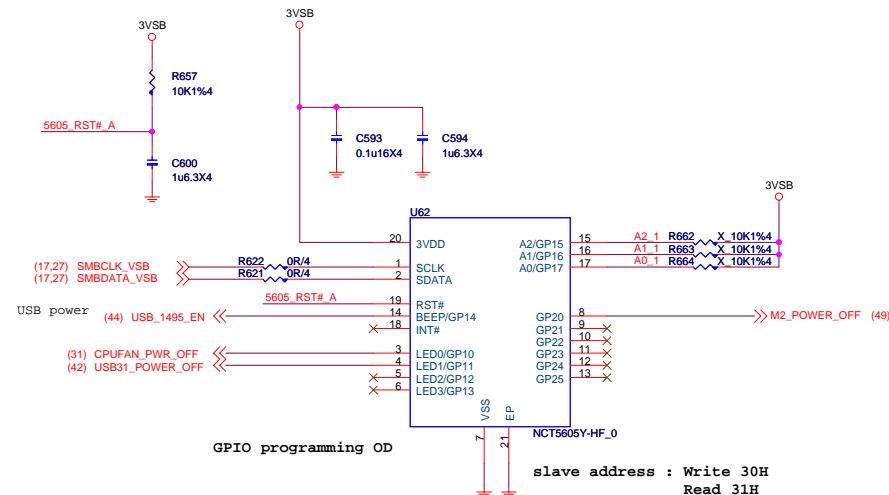
**SIO-NTC6792D/PS2**

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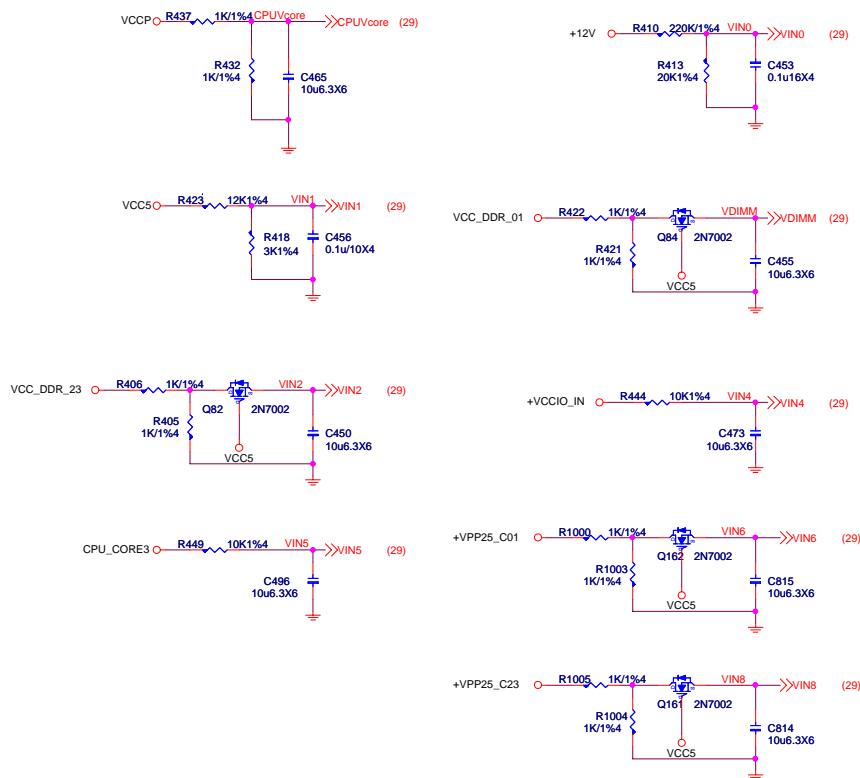
## PS2 KEYBOARD & MOUSE CONNECTOR



## CUT POWER CHIP

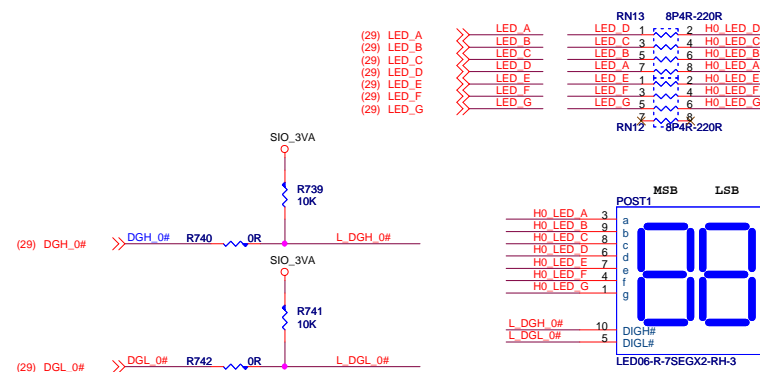


## HW Monitor - Voltage

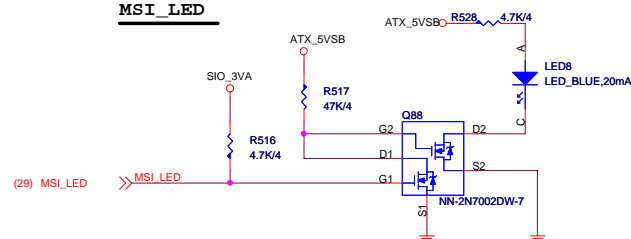


## DEBUG LED

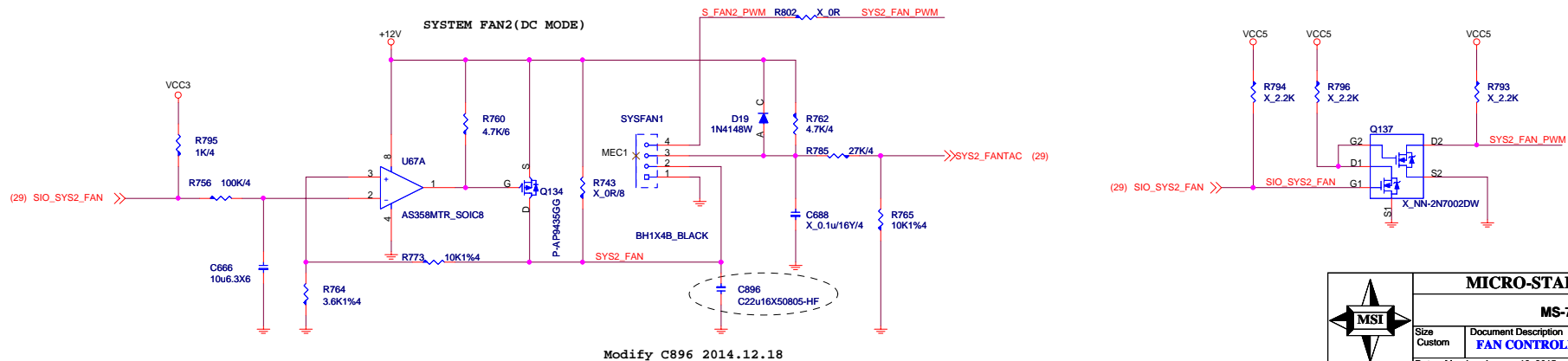
Placement一定要對  
(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)



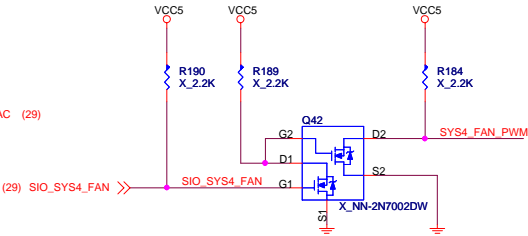
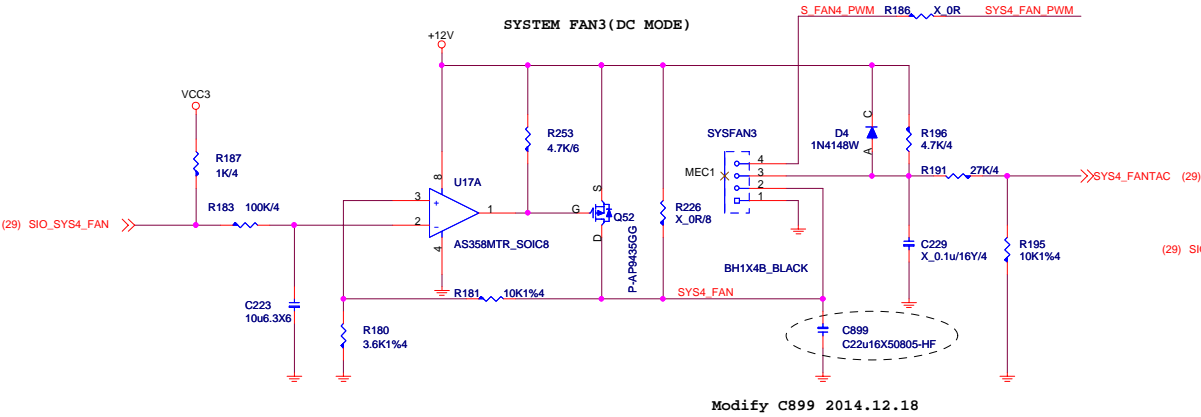
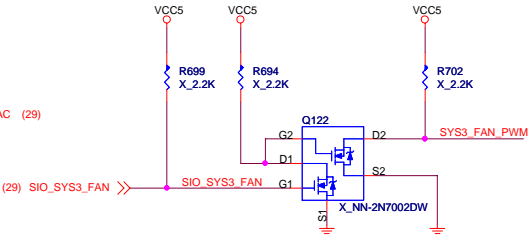
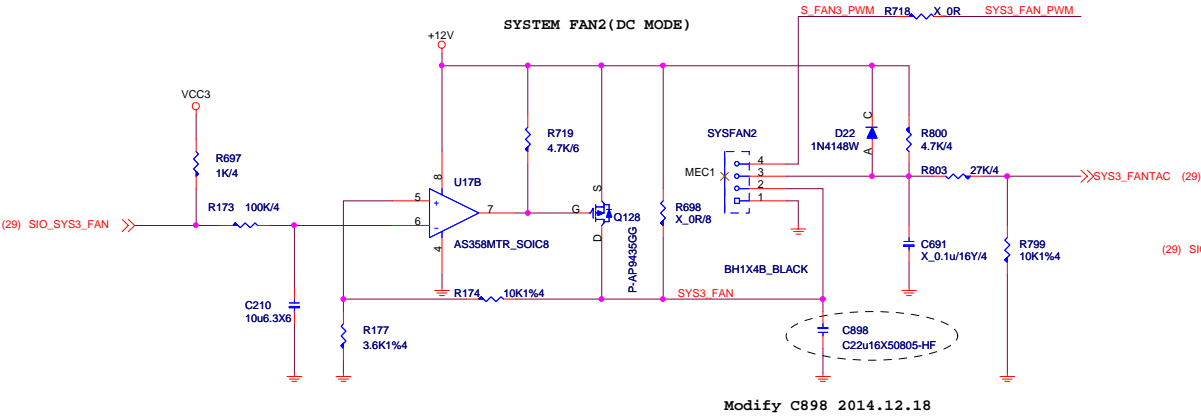
## MSI\_LED



**Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE )(FOR NCT6792)**

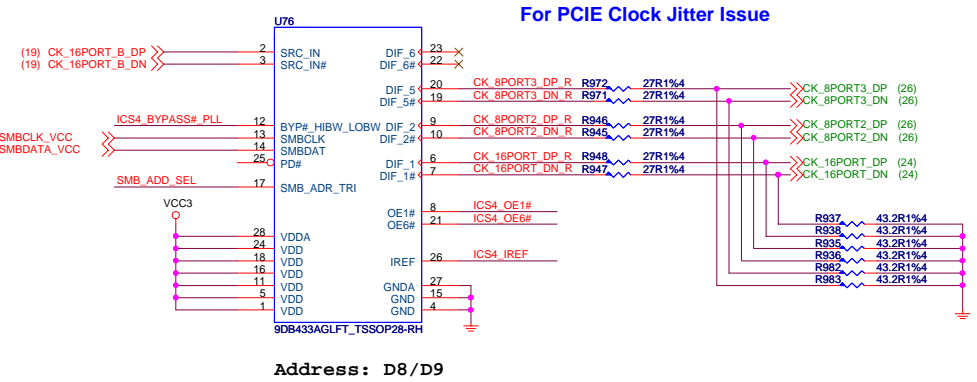
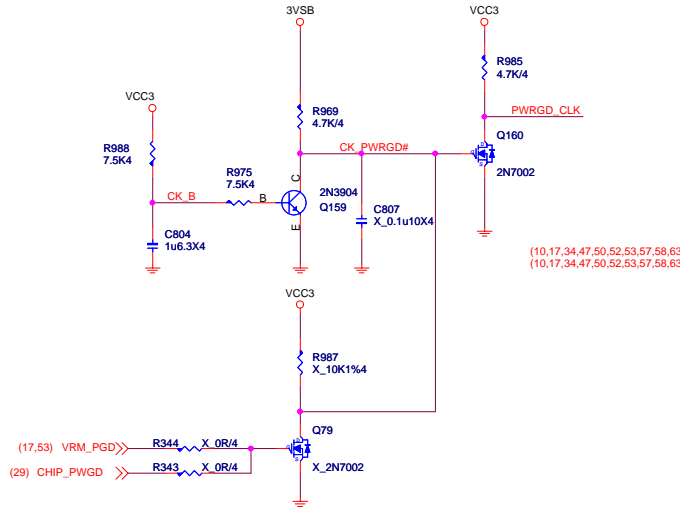
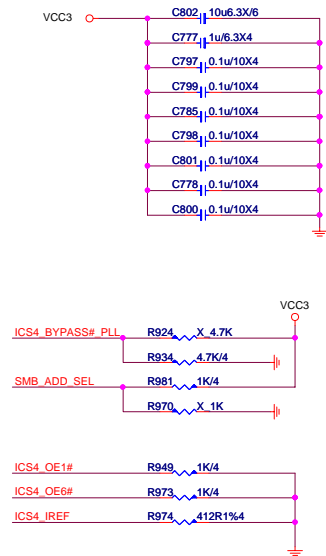


Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE )(FOR NCT6792)

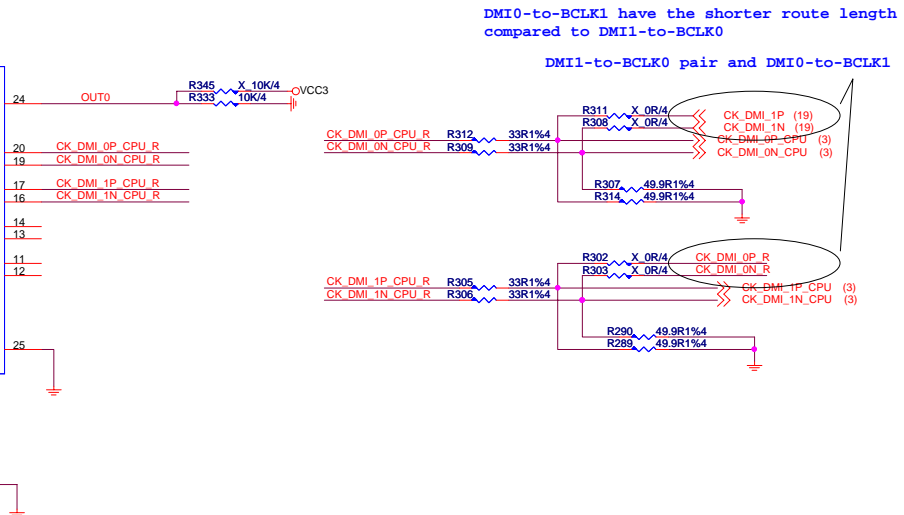
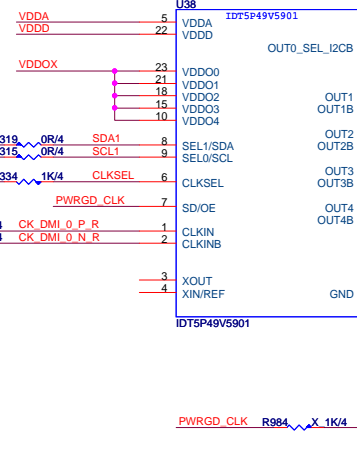
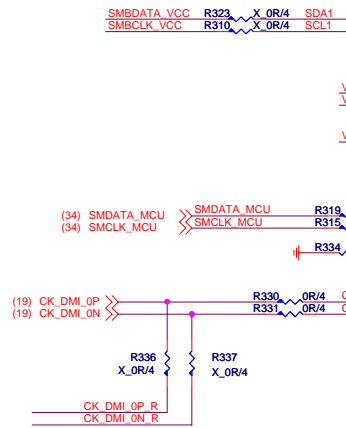
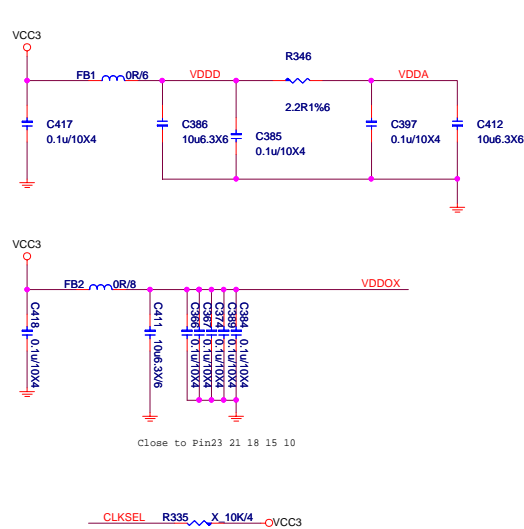




## CLK Buffer\_9DB433

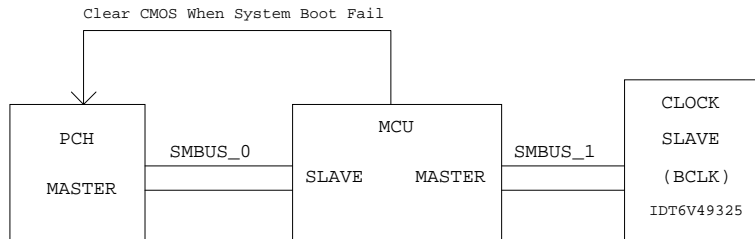
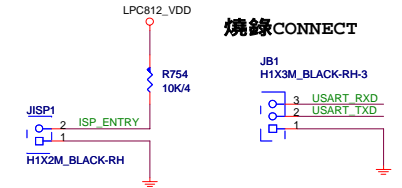
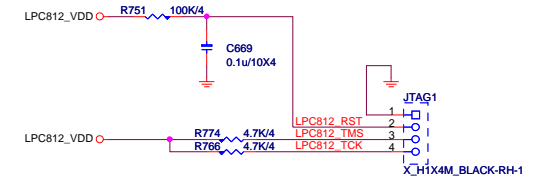
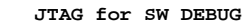
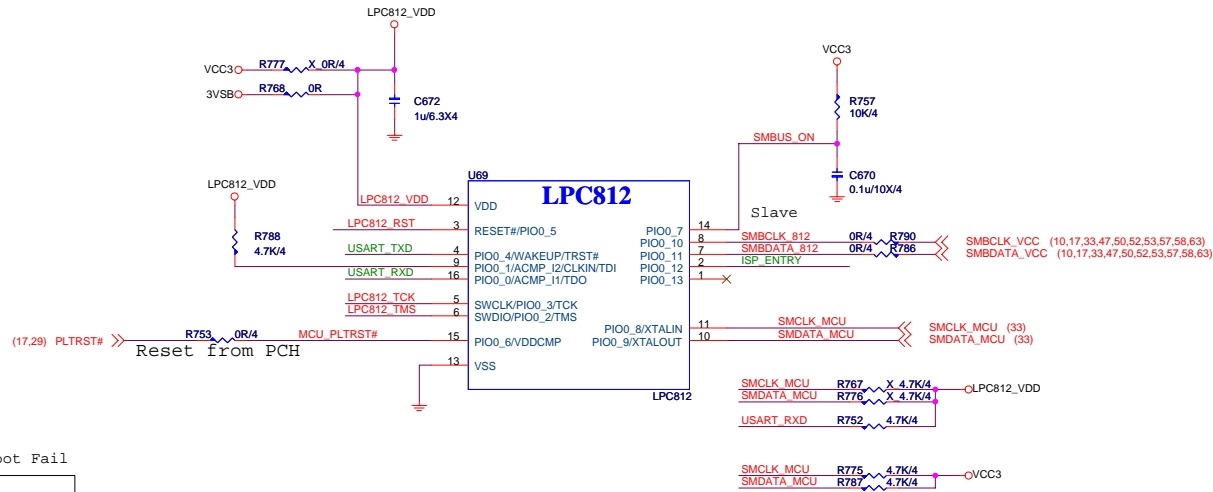


## CLK GEN-IDT5P49V5901

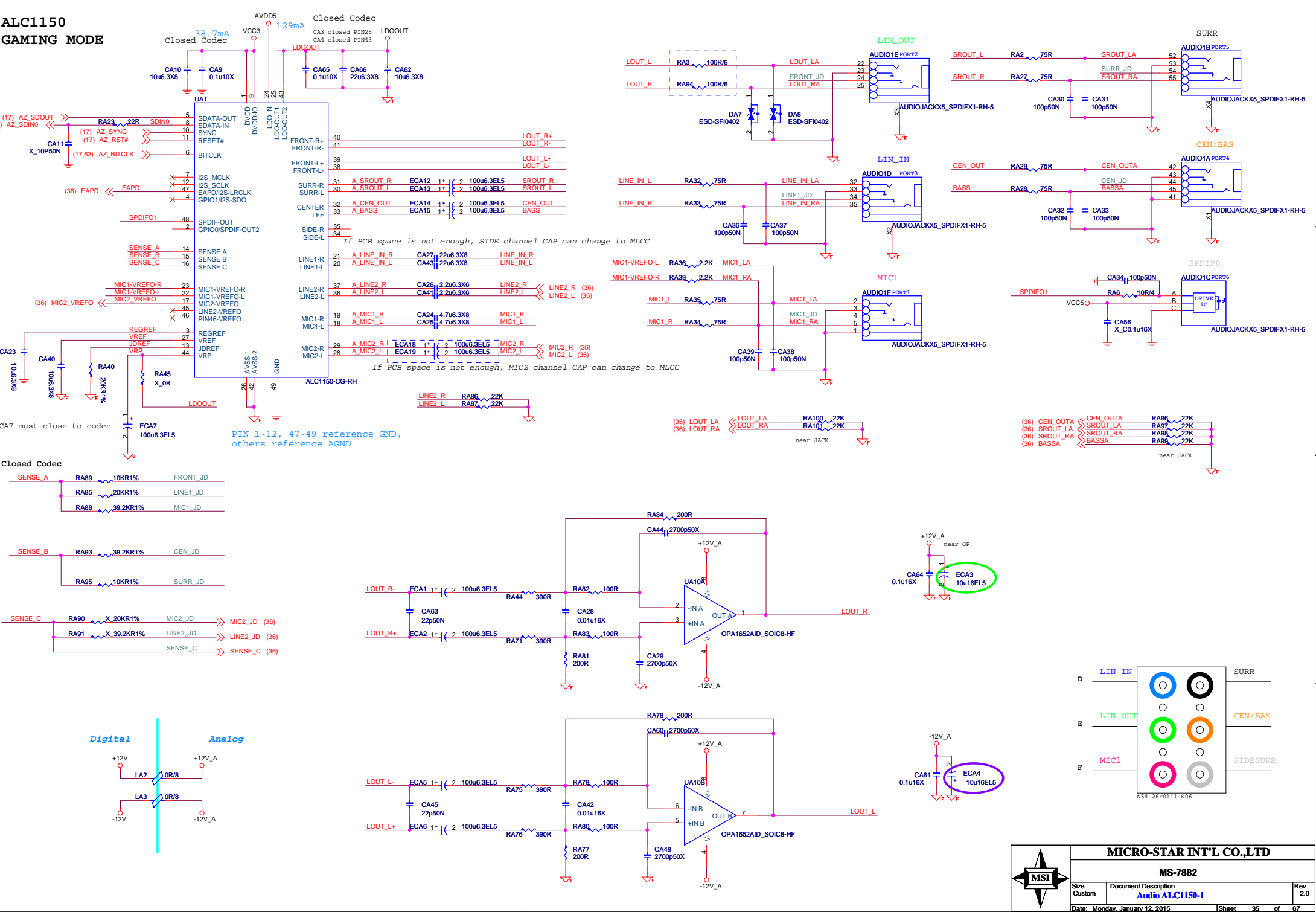


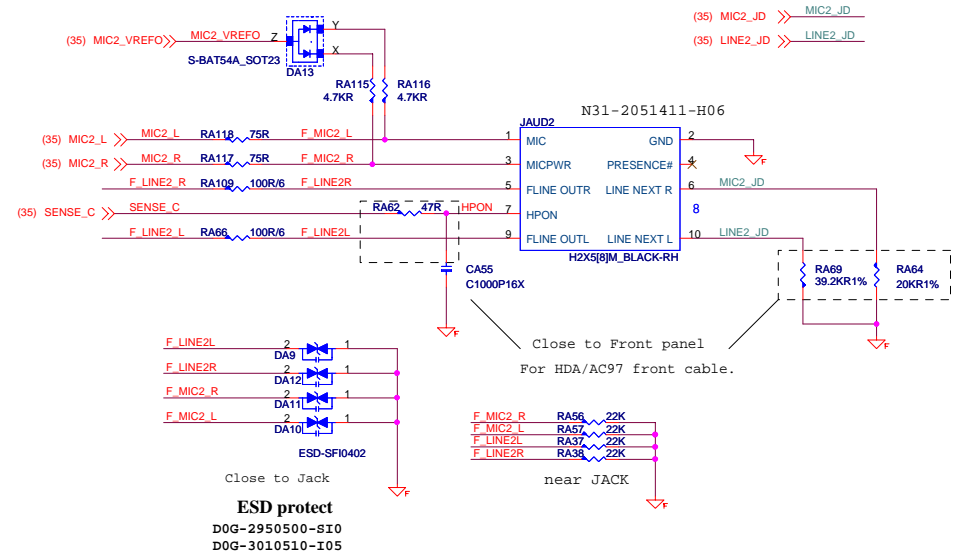
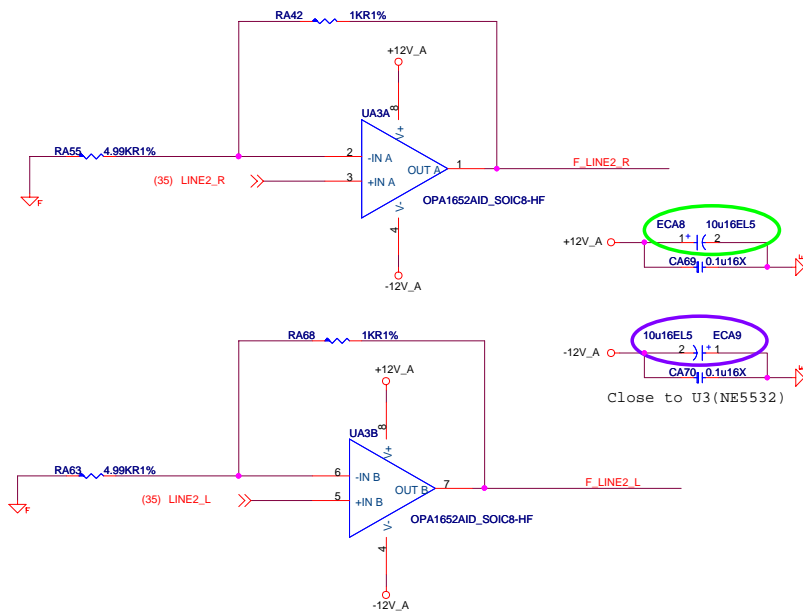
PIN:CLKSEL. Input clock select. Selects the active input reference source in manual switchover mode.  
 0 = XIN/REF, XOUT (default)  
 1 = CLKIN, CLKINB

```
SIO 6792 , GPIO13
default low , active high
```

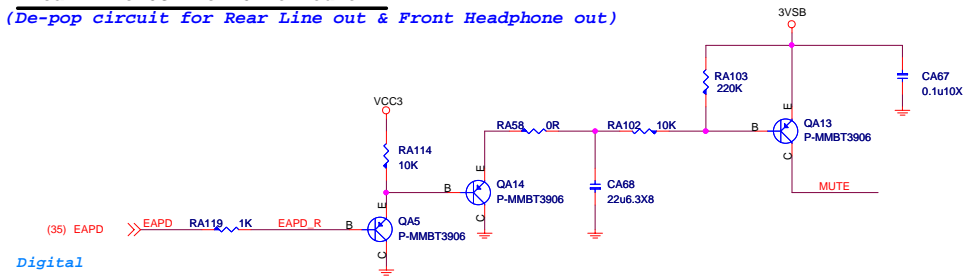


ALC1150  
GAMING MODE





### Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)

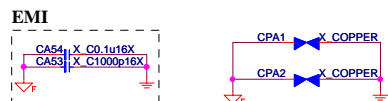
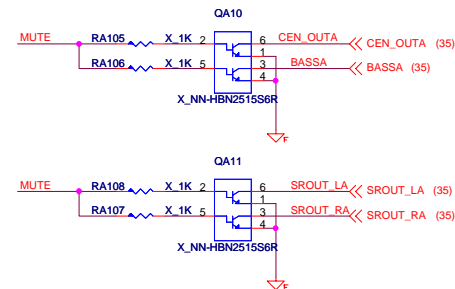


Digital

Analog

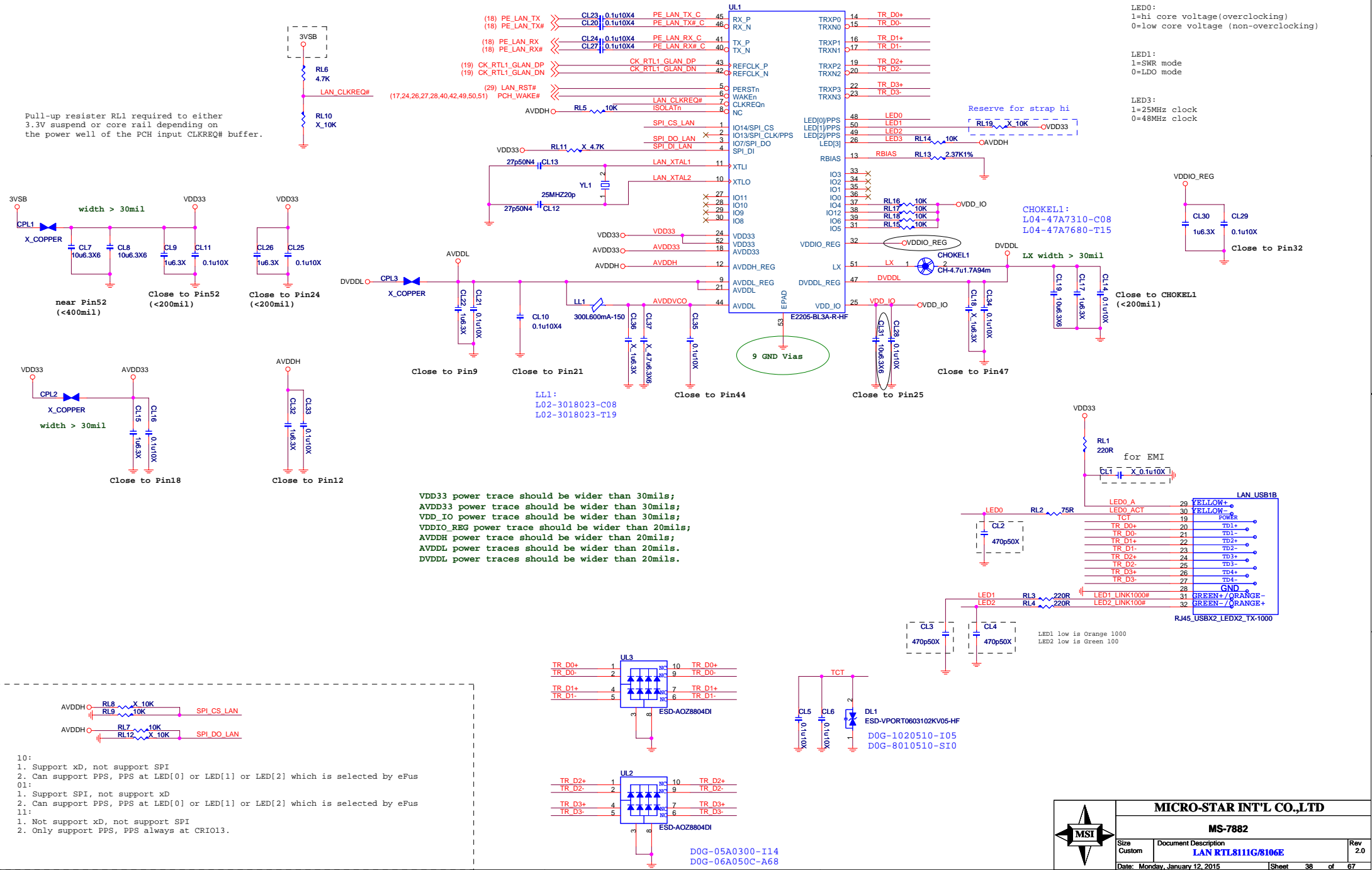


(add de-pop circuit by PM spec or customer request,  
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA23, CA24 to TVS)





# E2205-B Giga LAN



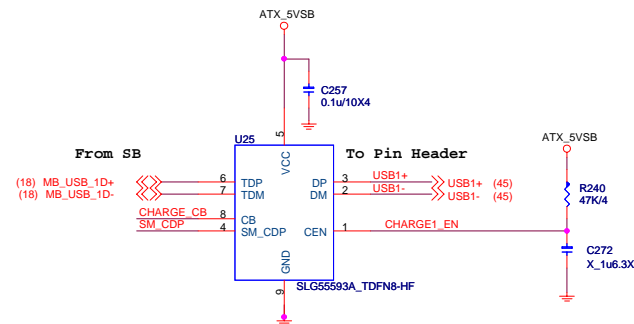
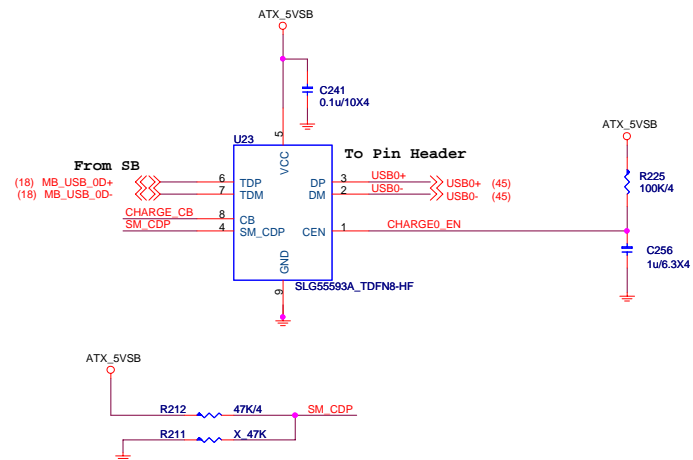


[illegible]

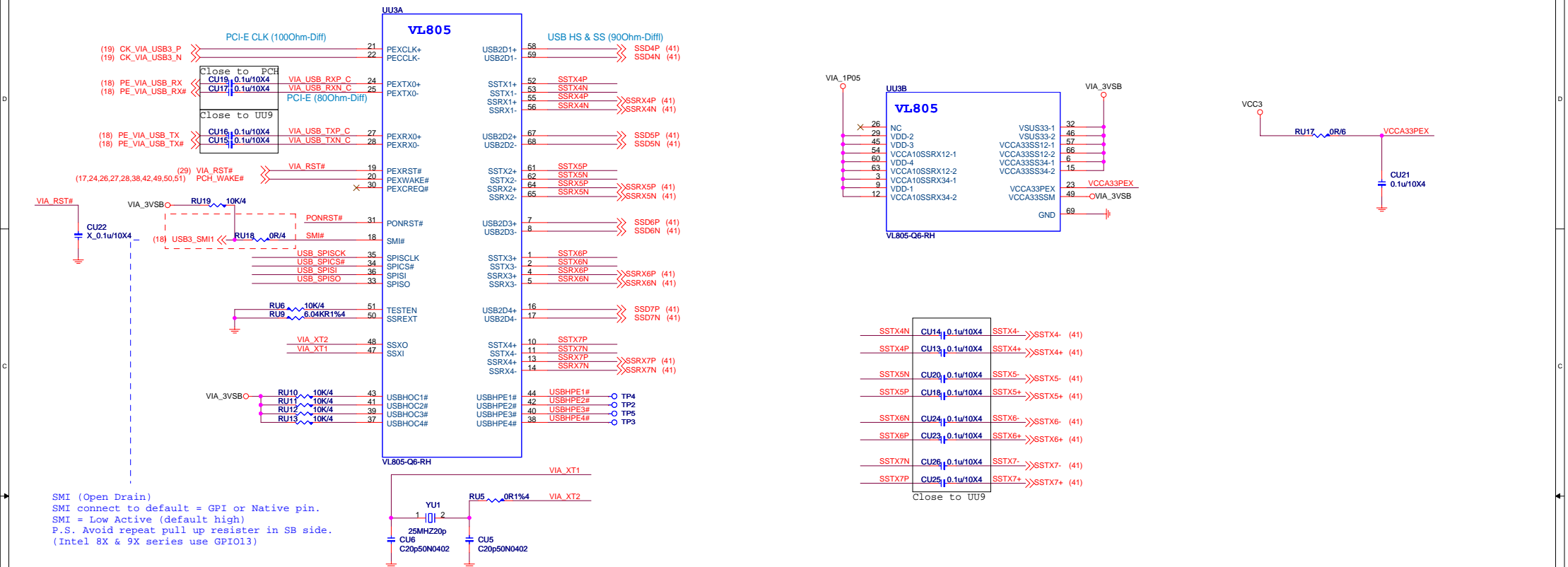
(29) CHARGE\_CB

Pin power : I\_3VSB  
Register power : I\_3VSB  
Register reset : I\_3VSB

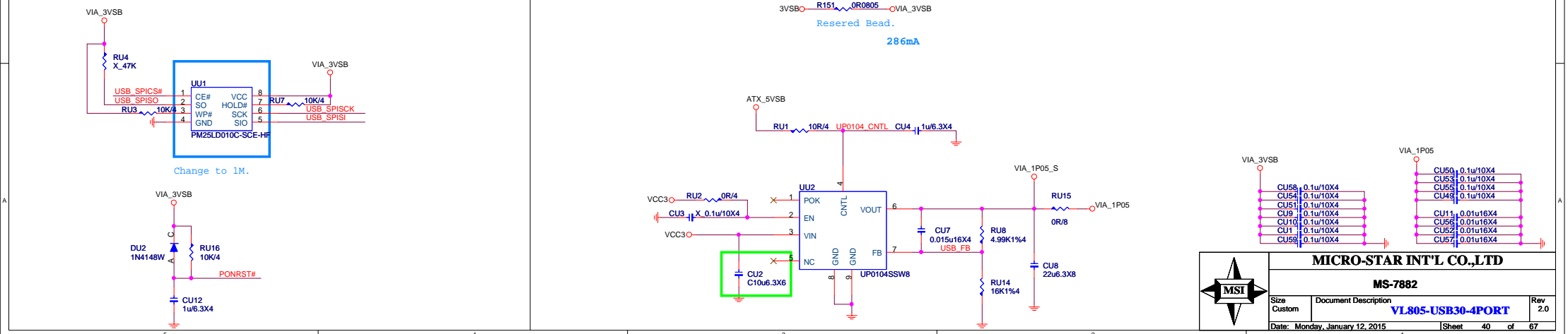
The diagram shows a MAX 2A voltage regulator. The input is 5V, connected to VIN1. The output is connected to a 100µF capacitor (C304) and a 100k resistor (X\_0.1u/100K4) to ground. The output is labeled IBC\_VCC1. The regulator is labeled MAX 2A and U33. The input is labeled CHARGE0\_EN and the output is labeled (18) OC#0.

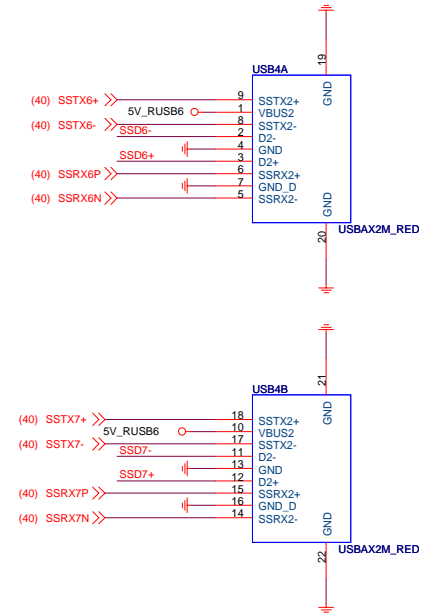
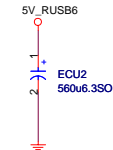
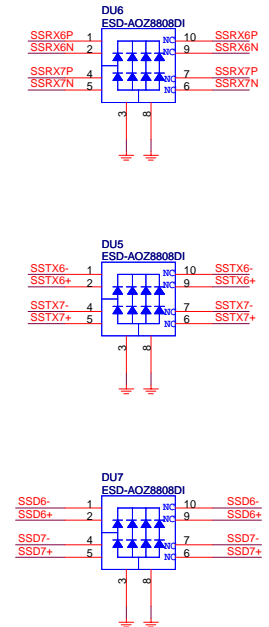
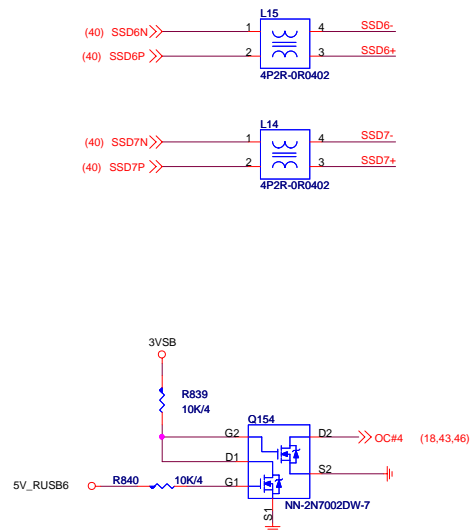
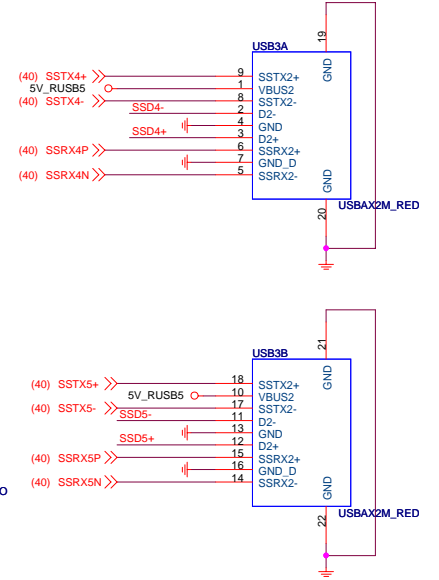
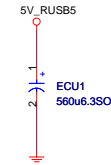
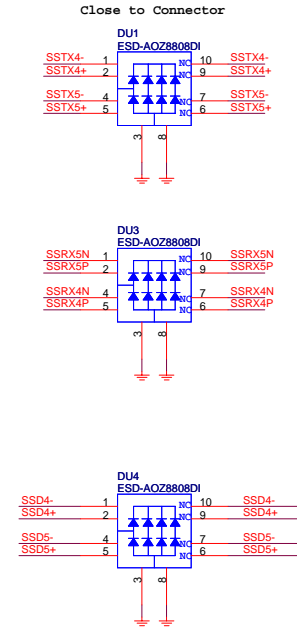
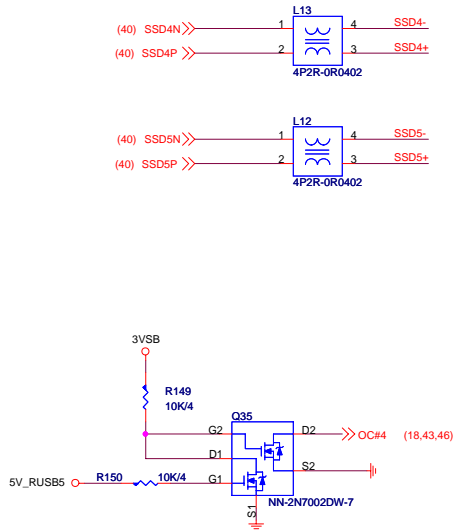


## VL805-USB30-4PORT



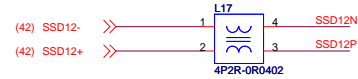
## EEPROM





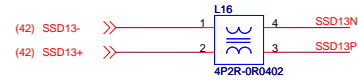


(42) SSTX12P >> SSTX12P CU37 0.22u6.3X4 SSTX12+  
(42) SSTX12N >> SSTX12N CU38 0.22u6.3X4 SSTX12-

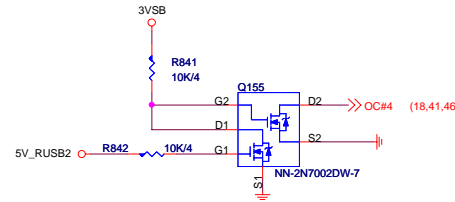


(42) SSRX12N >> SSRX12N  
(42) SSRX12P >> SSRX12P

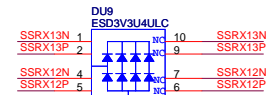
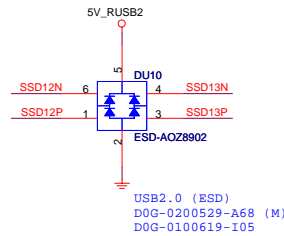
(42) SSTX13N >> SSTX13N CU35 0.22u6.3X4 SSTX13-  
(42) SSTX13P >> SSTX13P CU34 0.22u6.3X4 SSTX13+



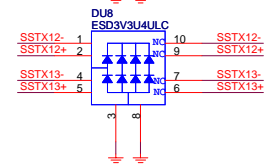
(42) SSRX13N >> SSRX13N  
(42) SSRX13P >> SSRX13P



### ESD Protection NEAR CONNECTOR

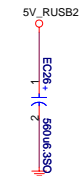
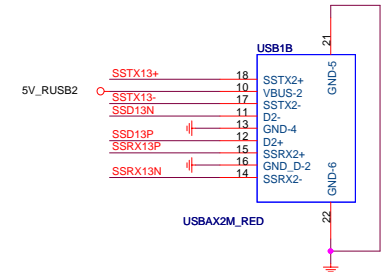
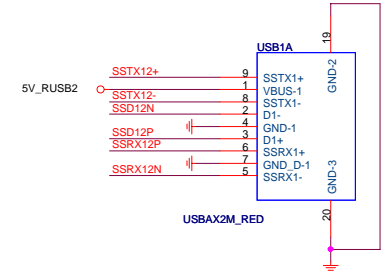


USB3.0 (ESD)  
D0G-06A050C-A68 (M)  
D0G-05A0300-I14



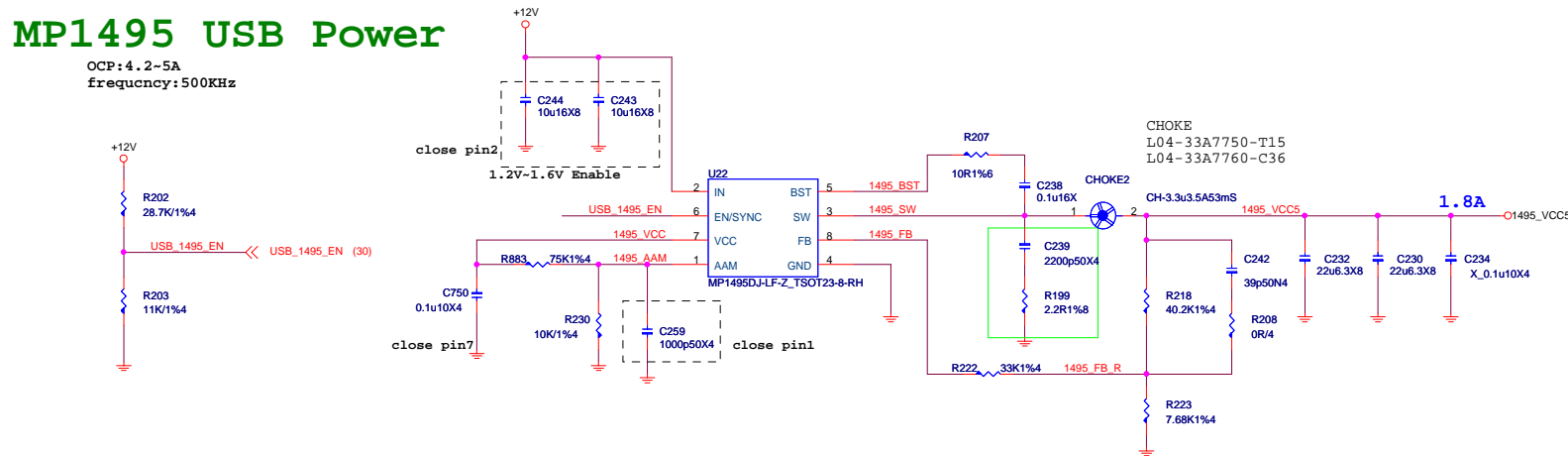
### Rear USB3 CONN

Important--  
If USB3.0 signal connect to front pin header,  
please must less than 0.6 inch, short trace  
has better eye diagram with some bad fly cable by SI customer.



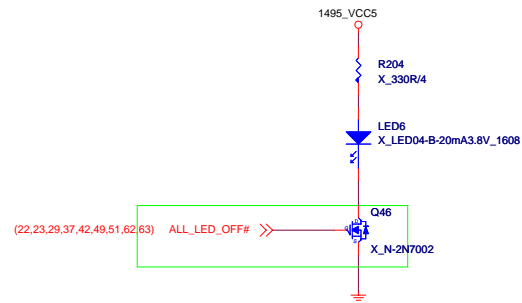
# MP1495 USB Power

OCP:4.2~5A  
frequency:500KHz

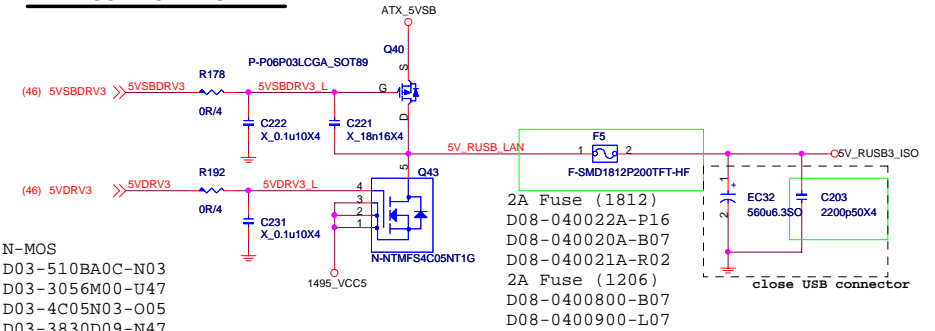


OC# signal connect to SB OC pin  
OC# can not be shared with other usb

## TO:NCT6792D GP17

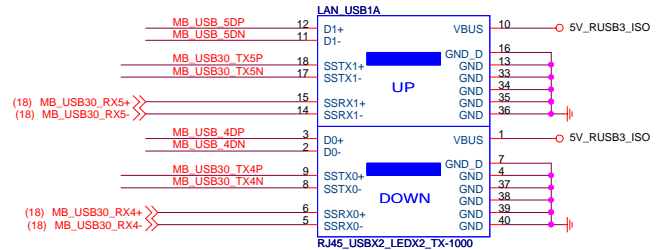
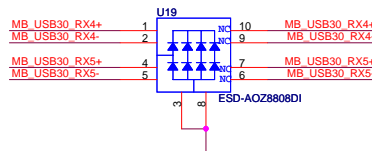
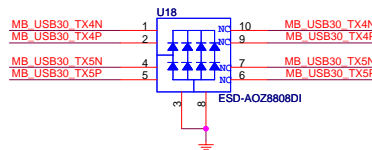
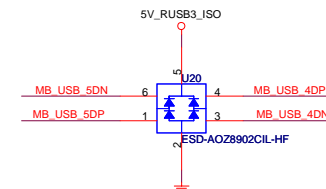
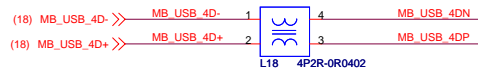


## REAR USB PORT POWER



(D03-P500303-N03 N/P MOS can replace Q1/Q2 )

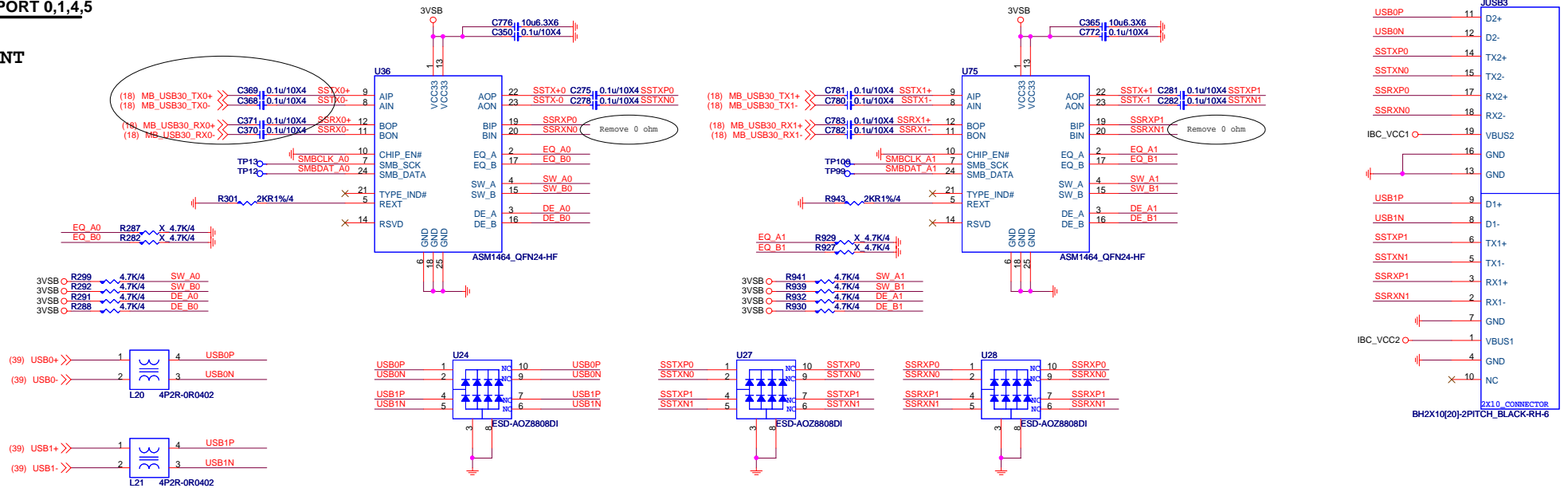
## USB3.0 Connector





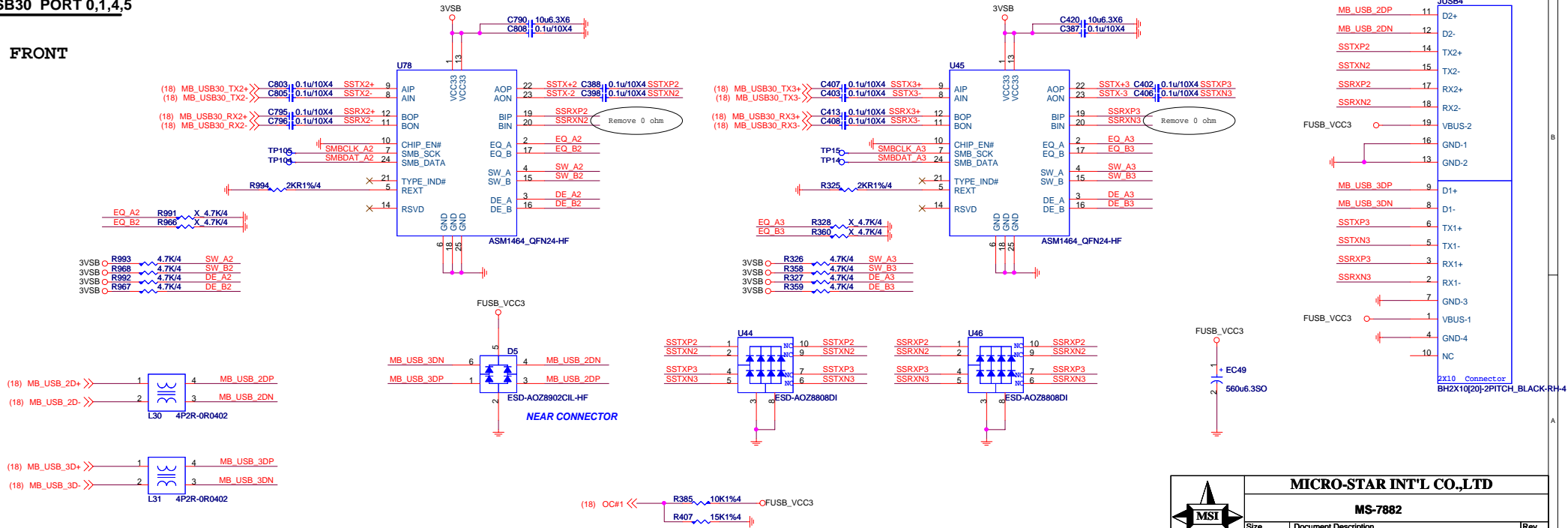
# FRONT USB30 PORT 0,1,4,5

## USB3.0 FRONT



# FRONT USB30 PORT 0,1,4,5

## USB3.0 FRONT

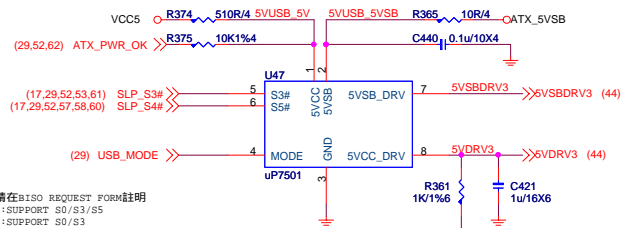


**MICRO-STAR INT'L CO.,LTD**

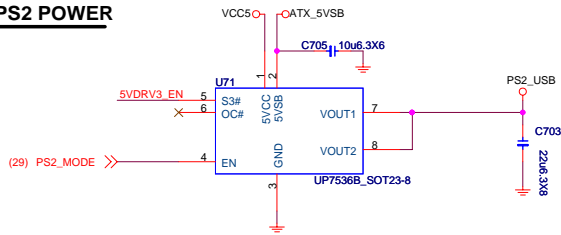
**MS-7882**

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Custom	USB3.0 FRONT	2.0
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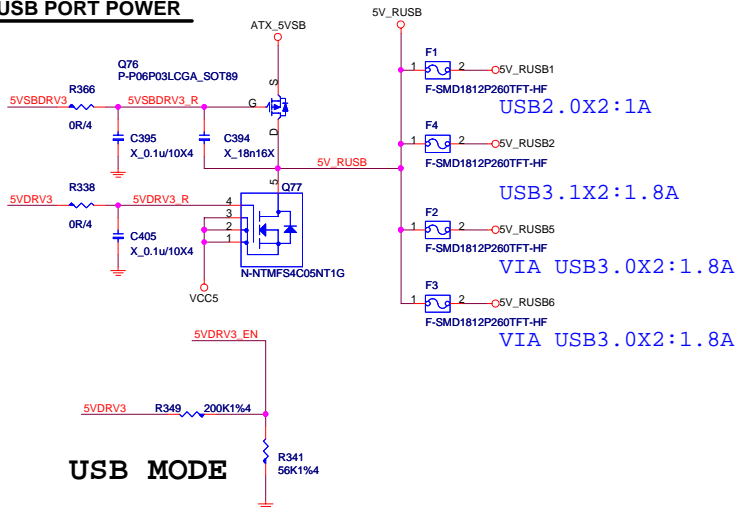
## USB POWER



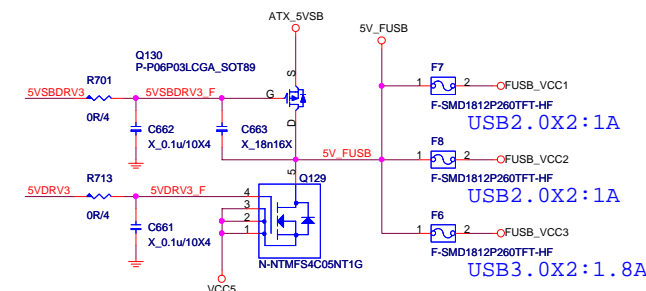
## PS2 POWER



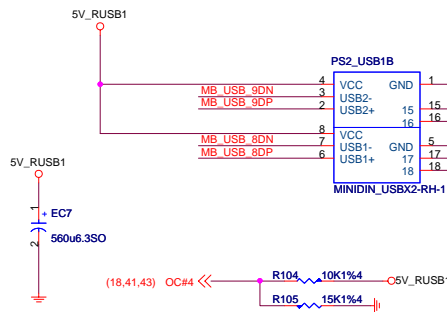
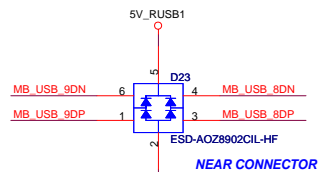
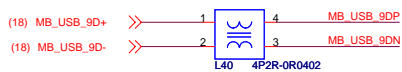
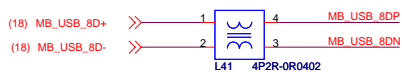
## REAR USB PORT POWER



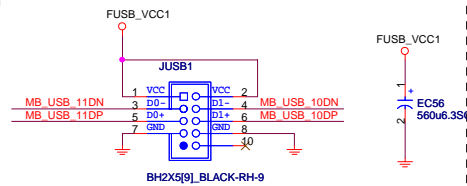
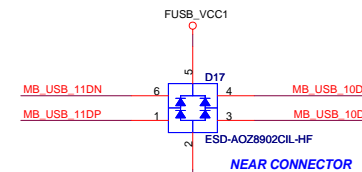
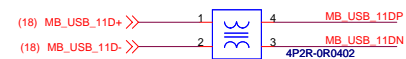
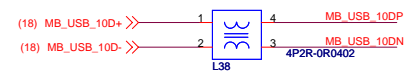
## Front USB PORT POWER



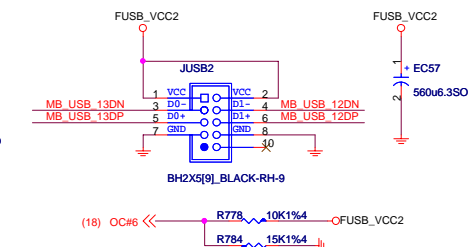
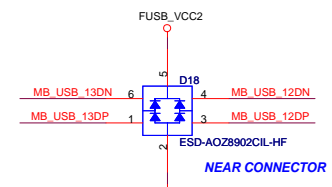
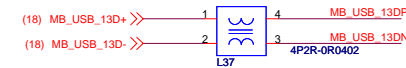
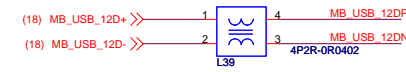
## REAR USB PORT 8,9 (With PS2)



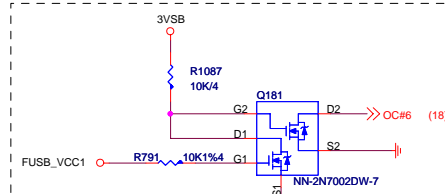
## FRONT USB PORT 10,11



## FRONT USB PORT 12,13



From OC5 to OC6  
Update 2014.12.30

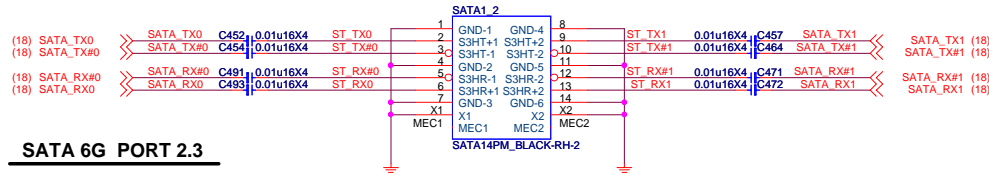


MICRO-STAR INT'L CO.,LTD

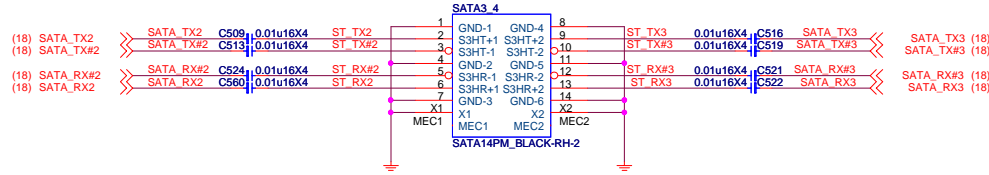
MS-7882

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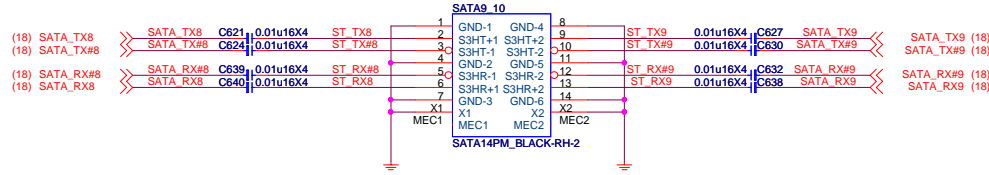
## SATA 6G PORT 0.1



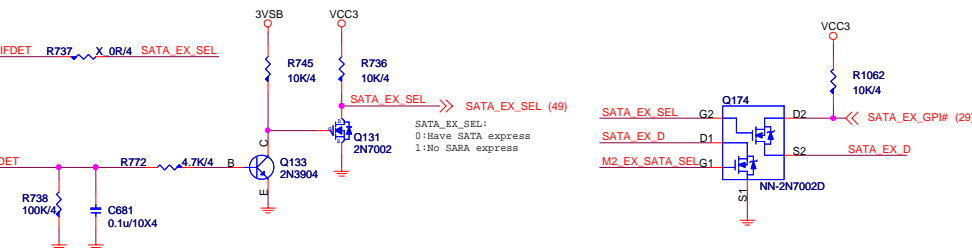
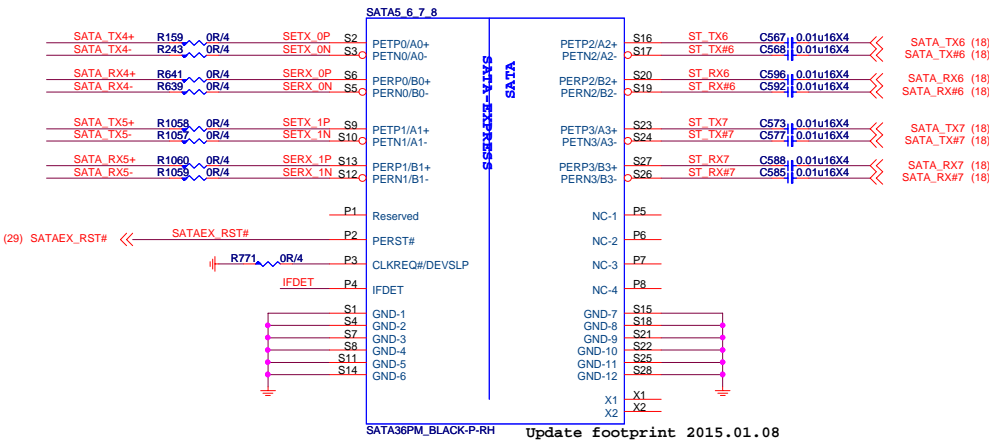
## SATA 6G PORT 2.3



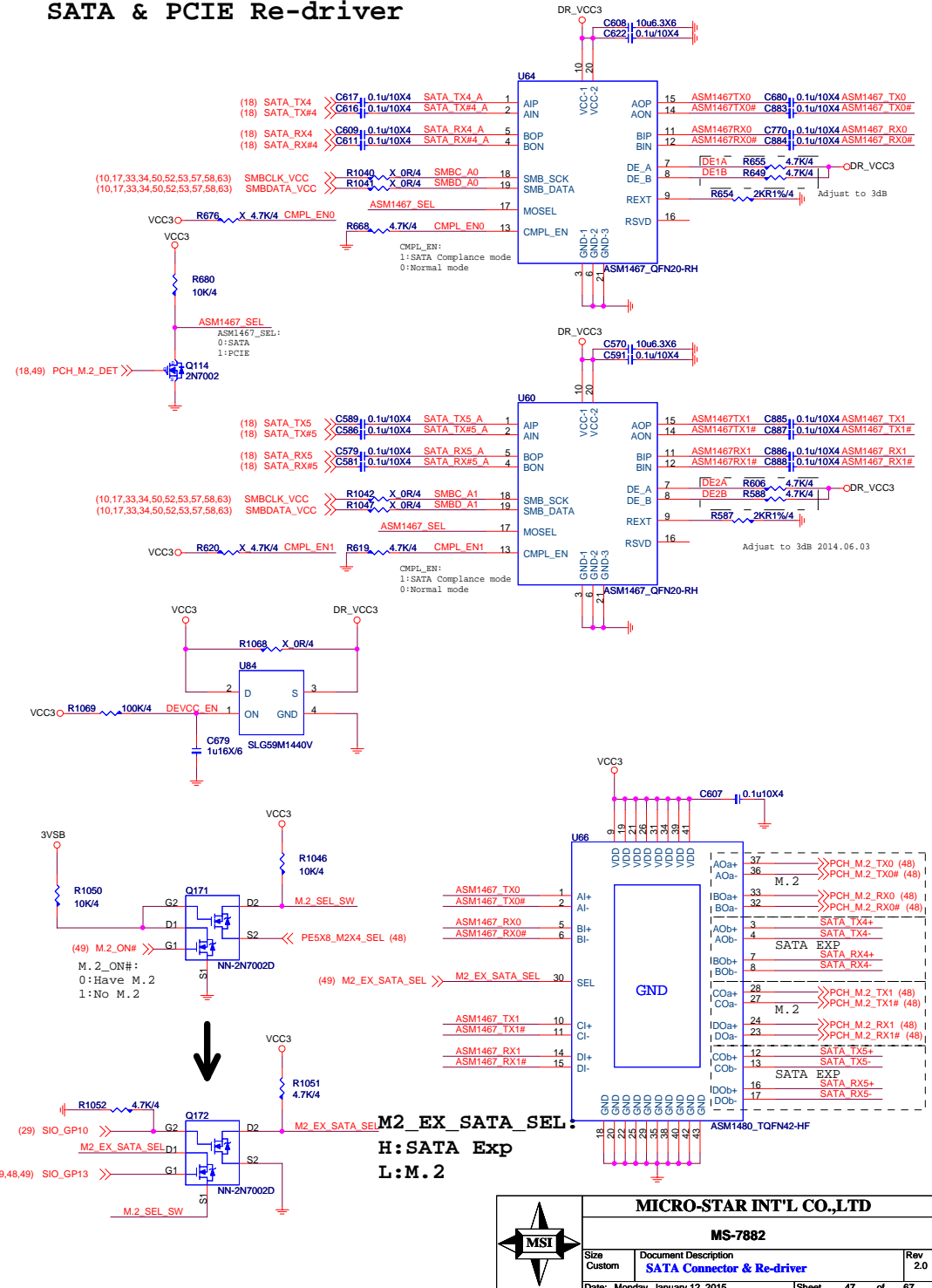
## SATA 6G PORT 8.9



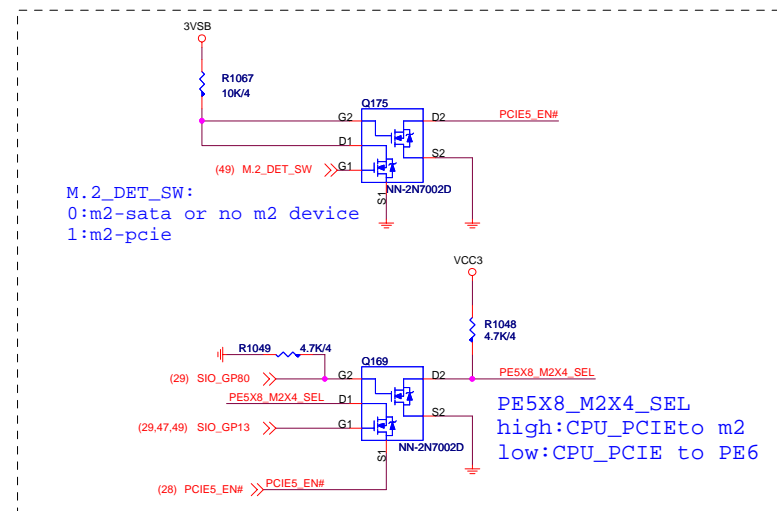
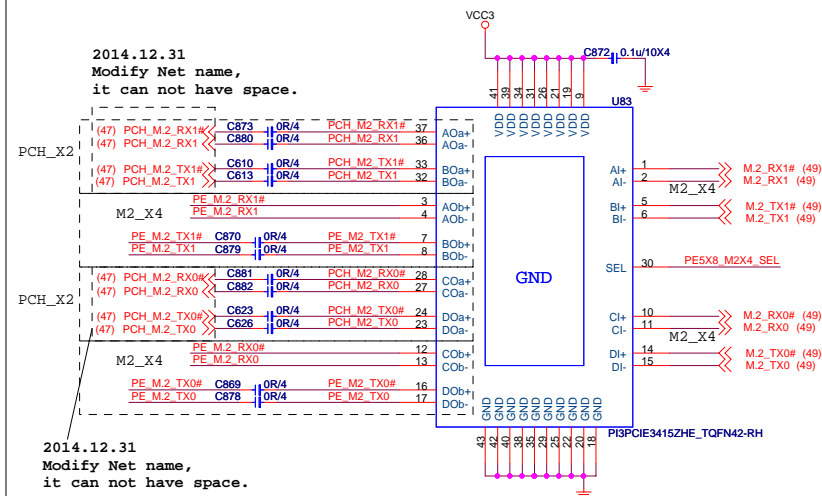
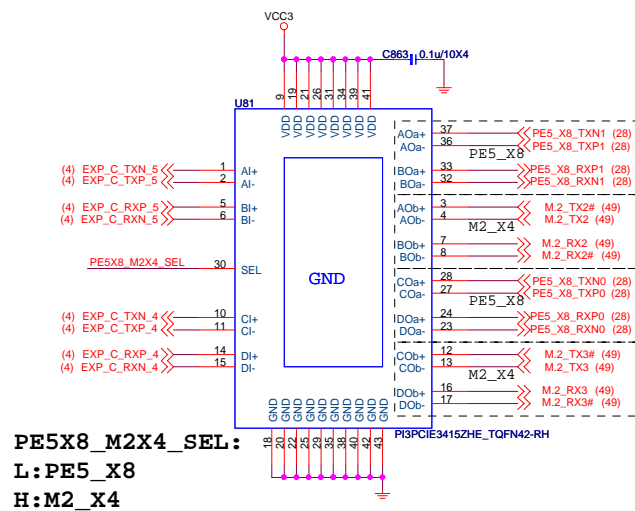
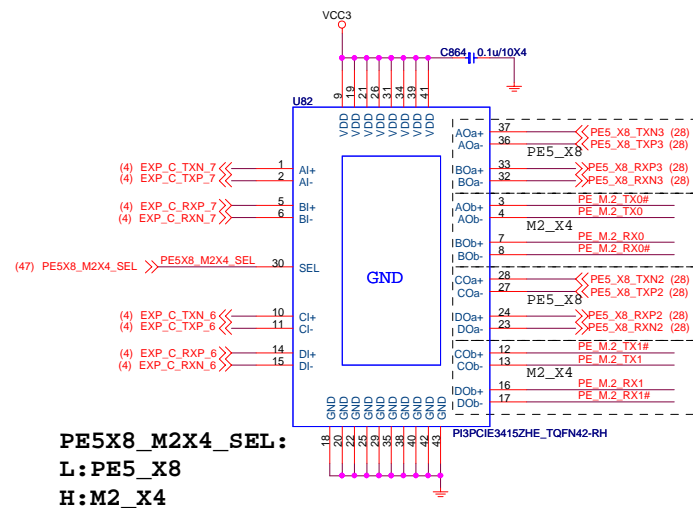
## SATA 6G PORT 4.5.6.7 & SATA Express



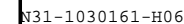
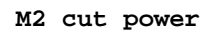
## SATA & PCIE Re-driver



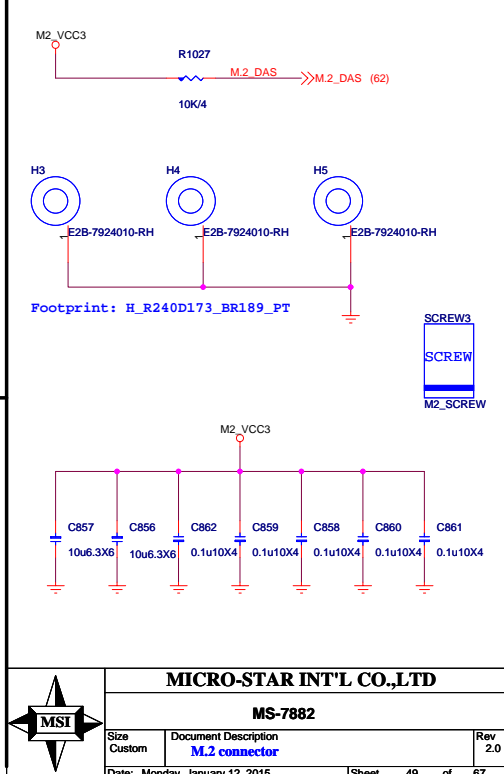
# PCIE5 & M.2 Switch



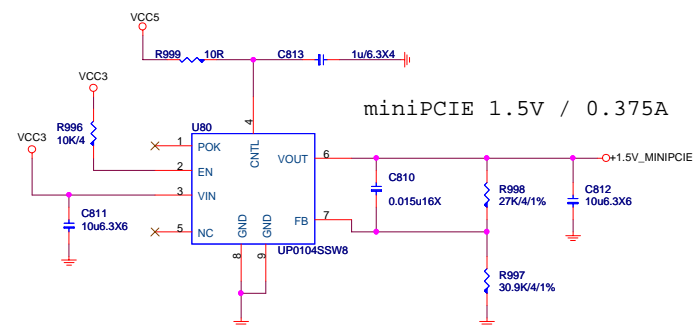
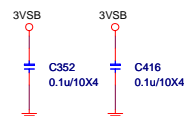
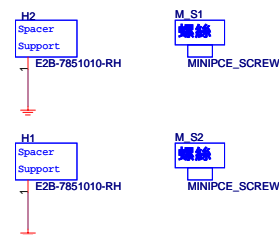
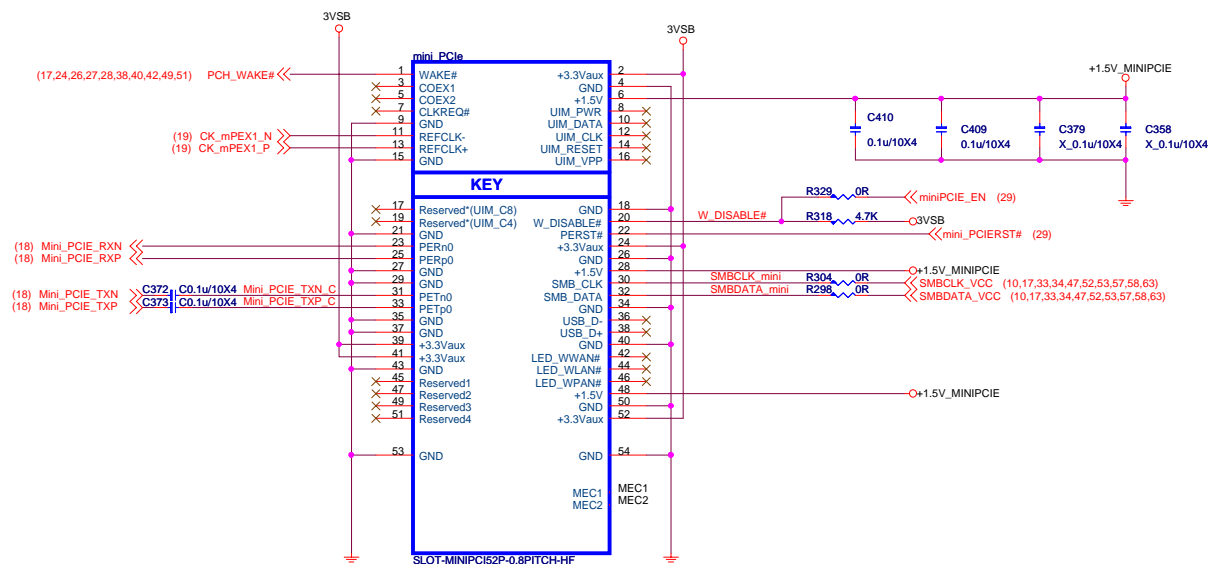
SIO_GP10	SIO_GP80	SIO_GP84	SIO_GP13	Mode
1	0	1:PCIE 0:SATA	0	M2-PCH
X	1	X	0	PCIEX8
X	0	X	0	M2-X4
0	X	1:PCIE 0:SATA	X	SATA Express
GPI(:0)	GPI(:0)	GPI(:0)	1	AUTO



```
For module card detect mode fail
```

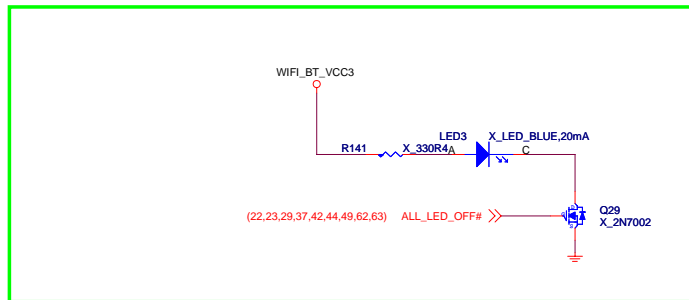
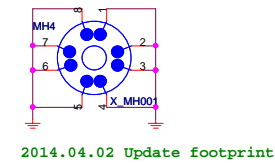
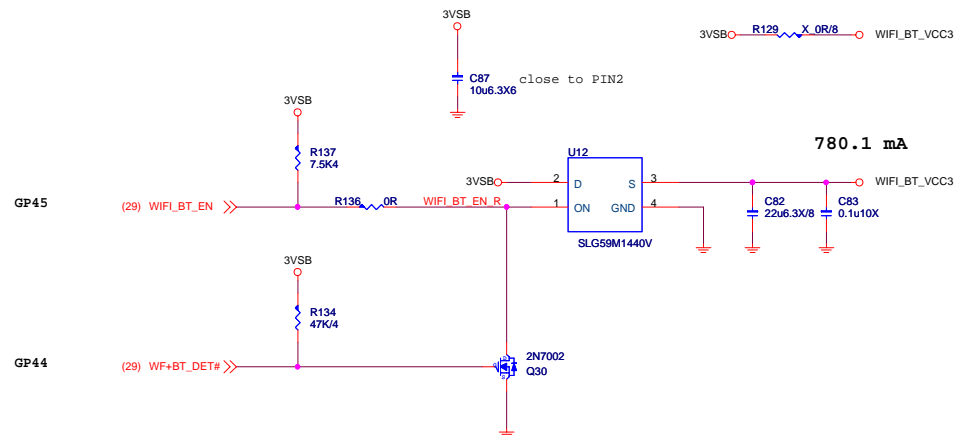
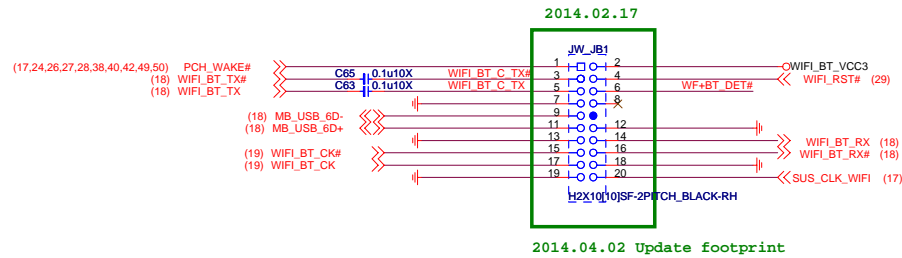


# mini PCIE



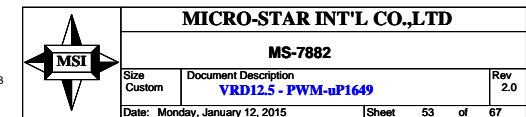
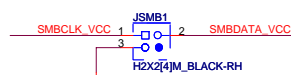
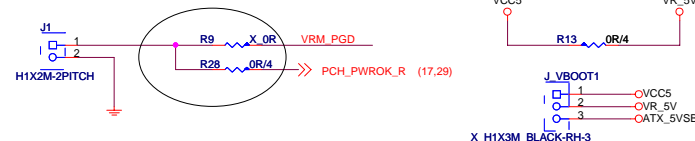


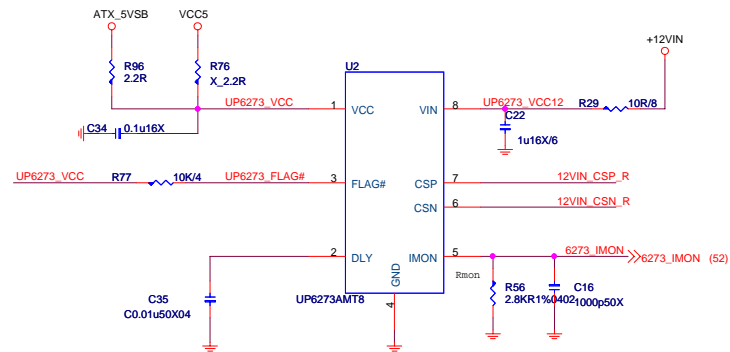
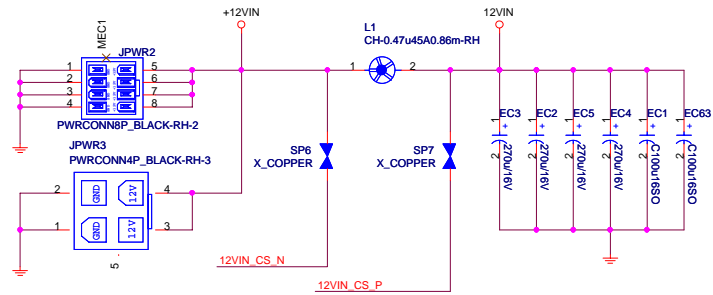
WIFI + Buletooth





**VCCP\_1.8V 180A, OC margin 2.5V=240A  
OCP:336A for 8Phase**





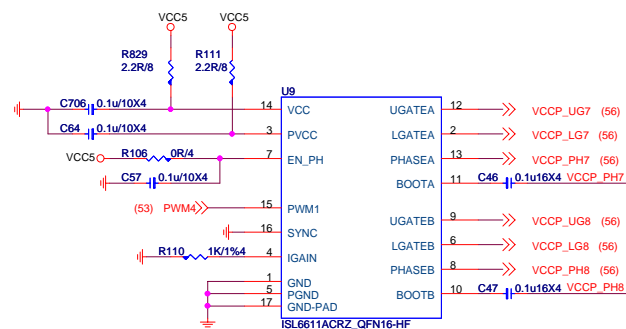
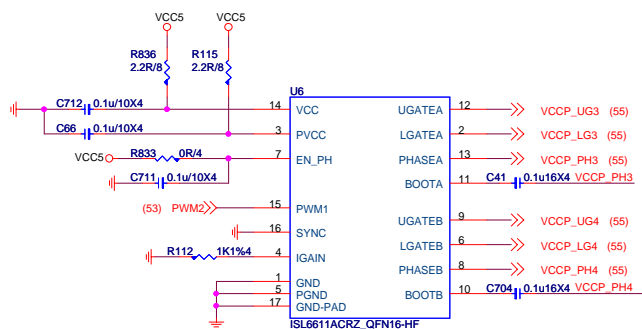
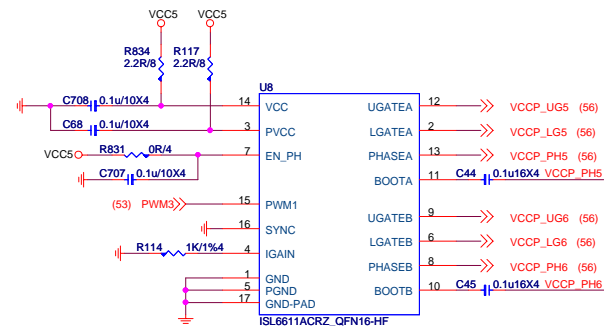
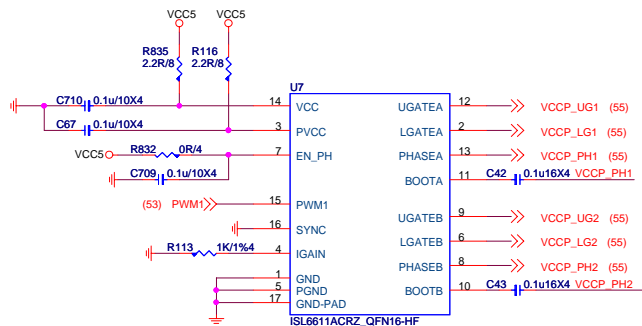
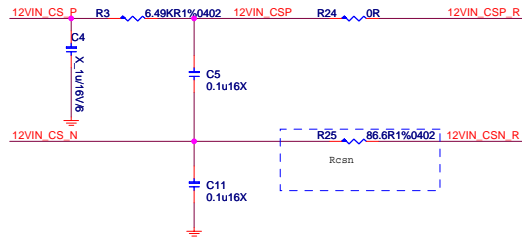
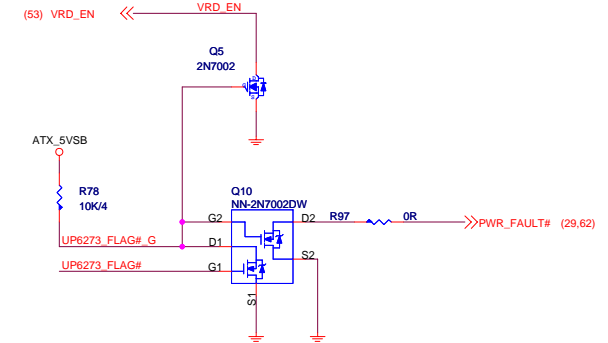
OCP: 39A

$$I_{in} = (V_{mon} \cdot R_{csn}) / (R_{mon} \cdot R_{dc})$$

$$V_{mon} = 1.2$$

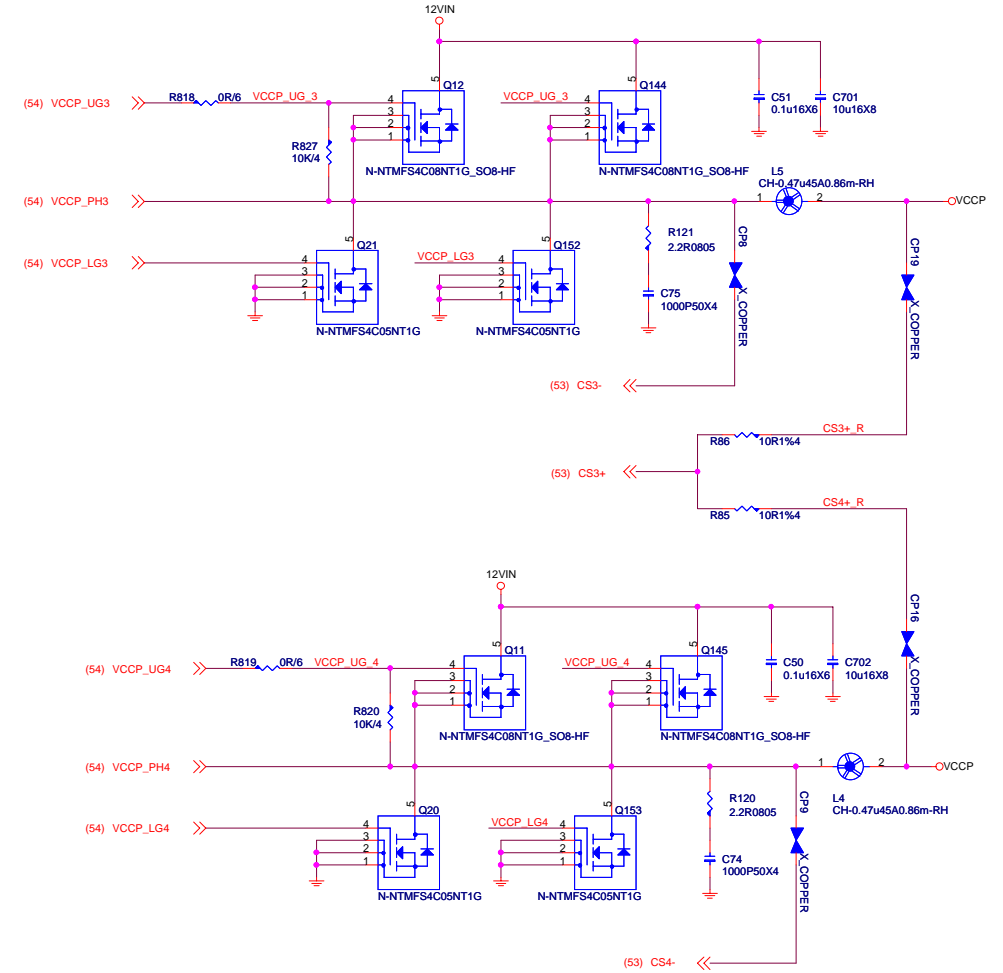
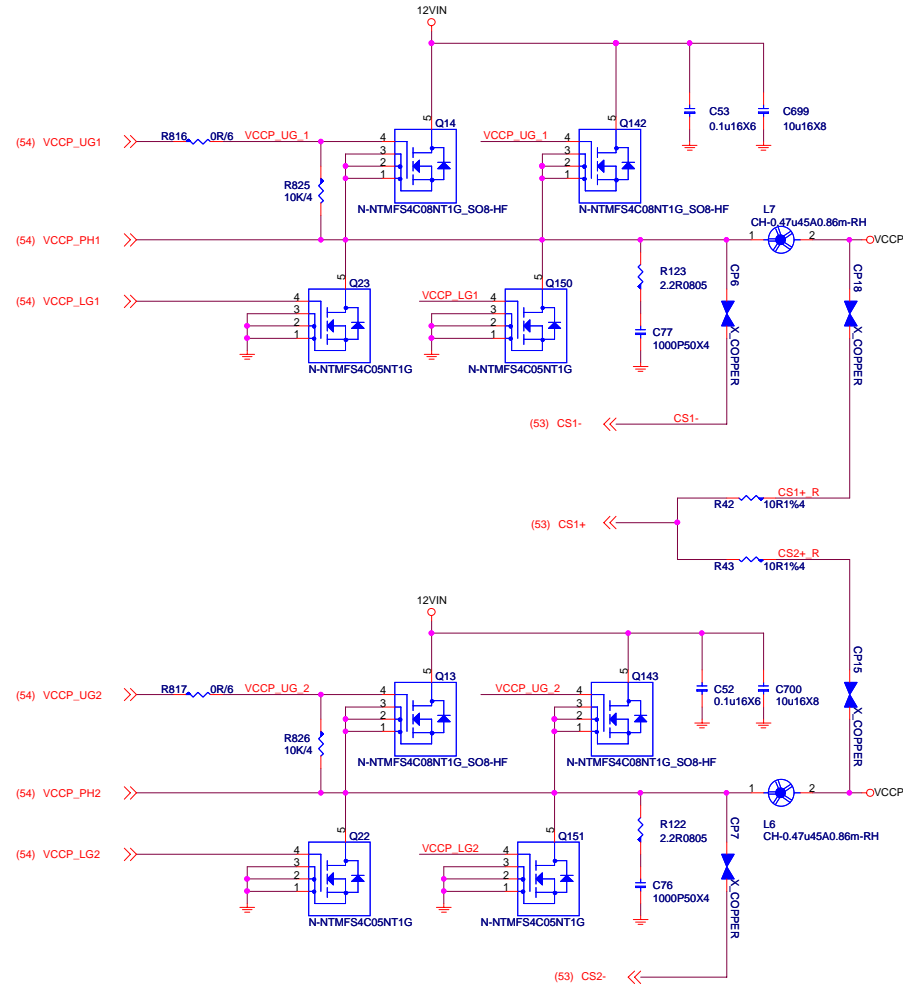
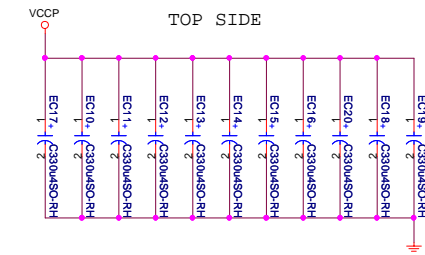
can change OCP trigger level by Rcsn and Rmon

$$(1.2 * 0.2) / (10K * 0.3m) = xx A$$



$$I_{rms} = I_{out} \sqrt{D/N - (D)^2} = 320 \sqrt{0.02 - (0.16)^2} = 23.94A$$

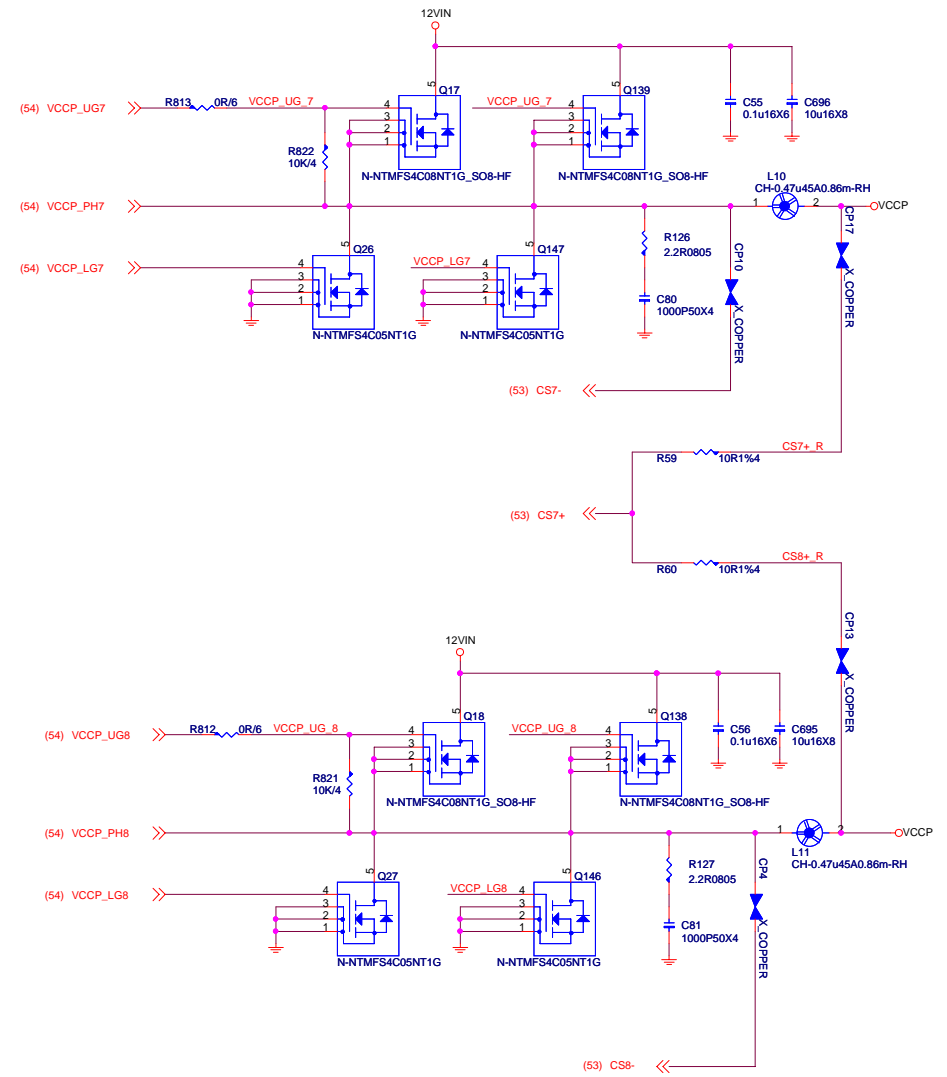
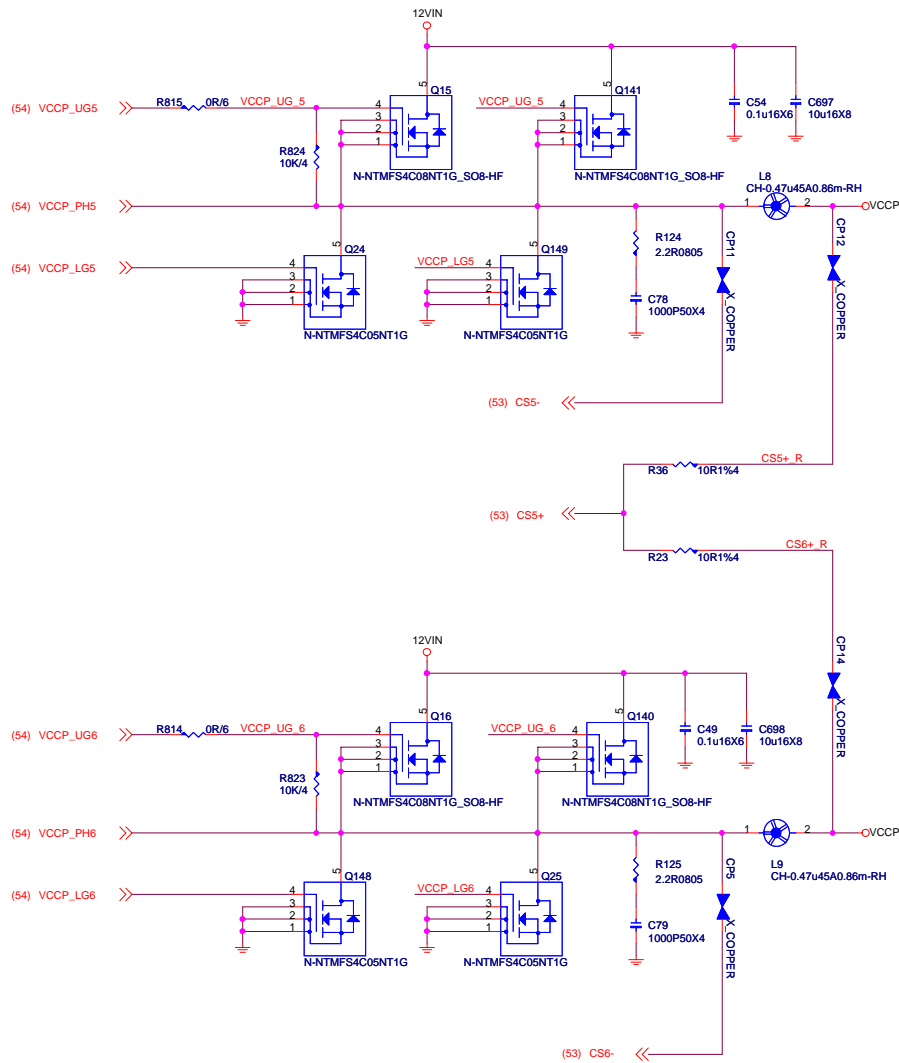
$$5000mA * 5 = 25A > 23.94A$$



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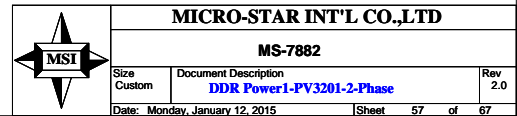
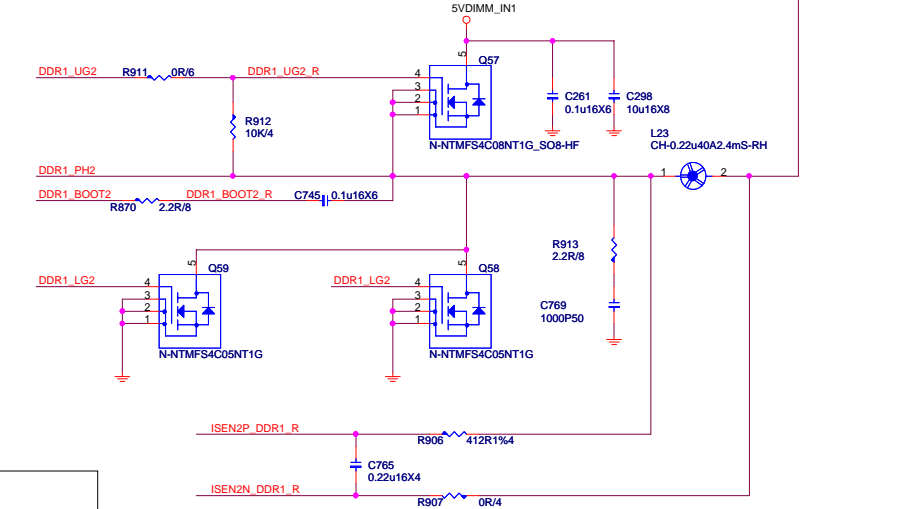
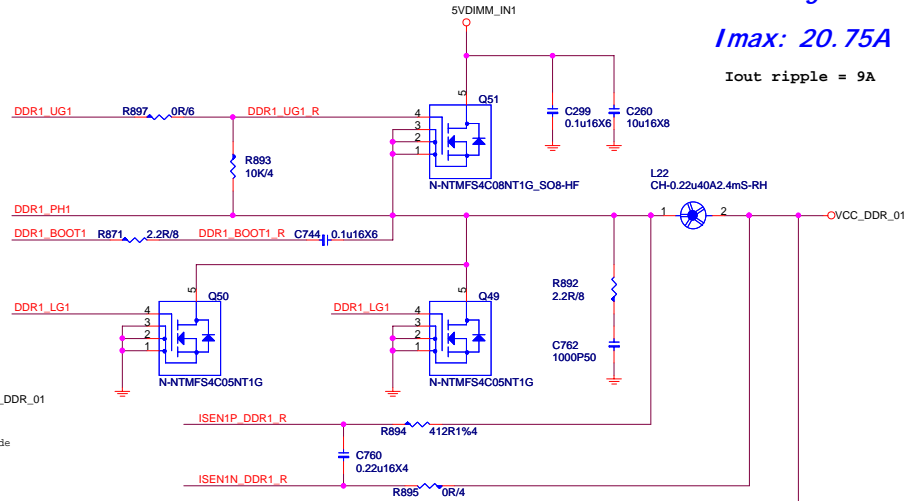
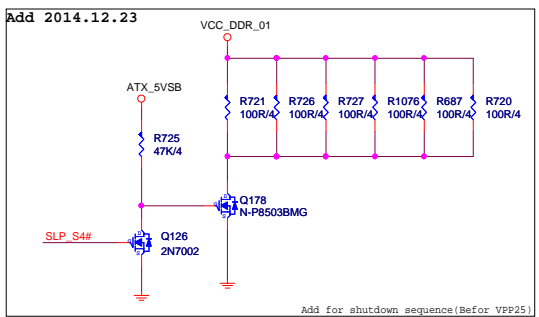
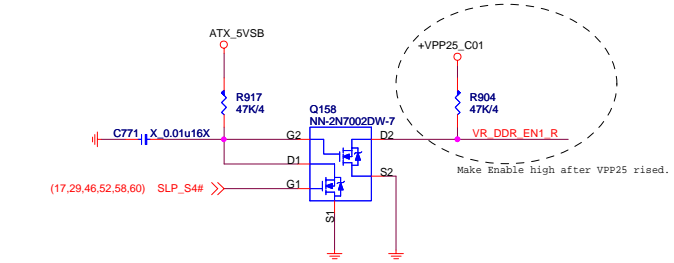
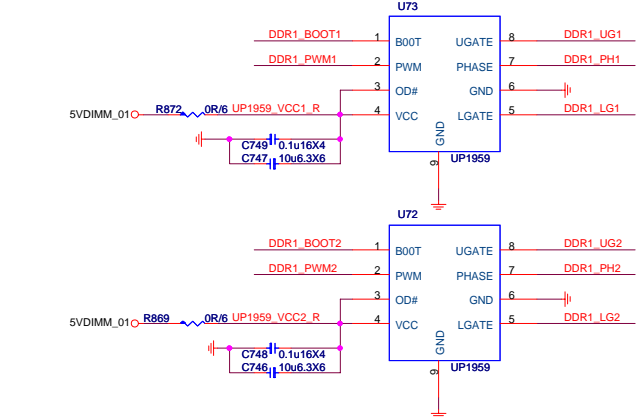
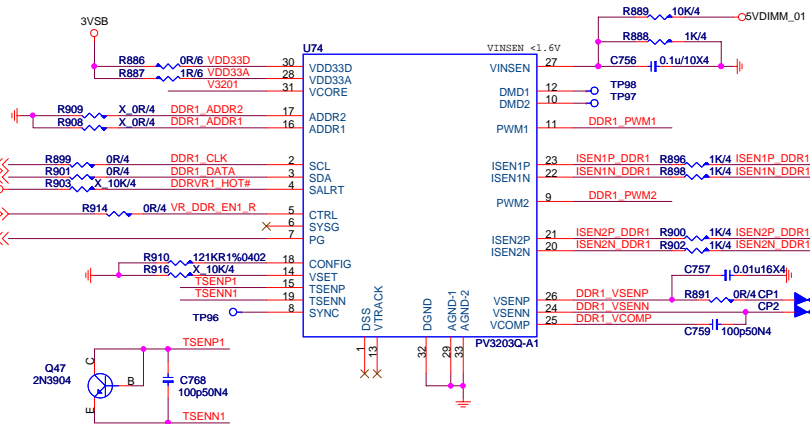
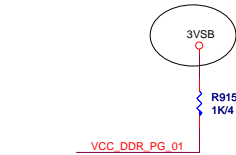
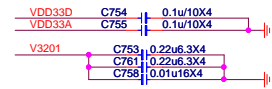
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**DDR4\_1.2V 11A, OC margin=44A**  
**OCP:66A for 2Phase**

$OCP = 64A$   
 $OC \text{ margin} = 44A$   
 $I_{max} = 20.75A$   
 $I_{out \text{ ripple}} = 9A$



DDR Power1-PV3203-2-Phase

DDR4\_1.2V 11A, OC margin=44A

OCP:66A for 2Phase

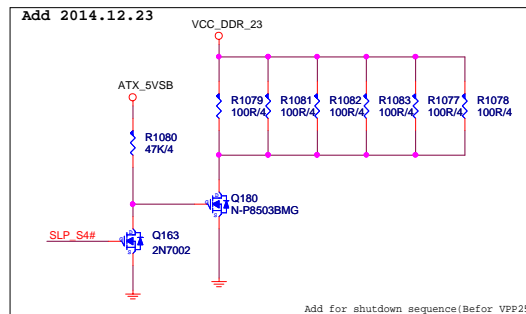
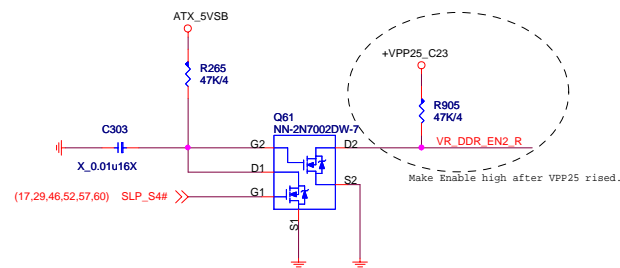
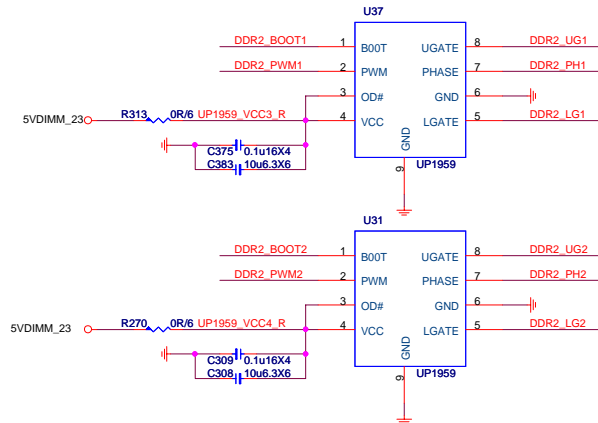
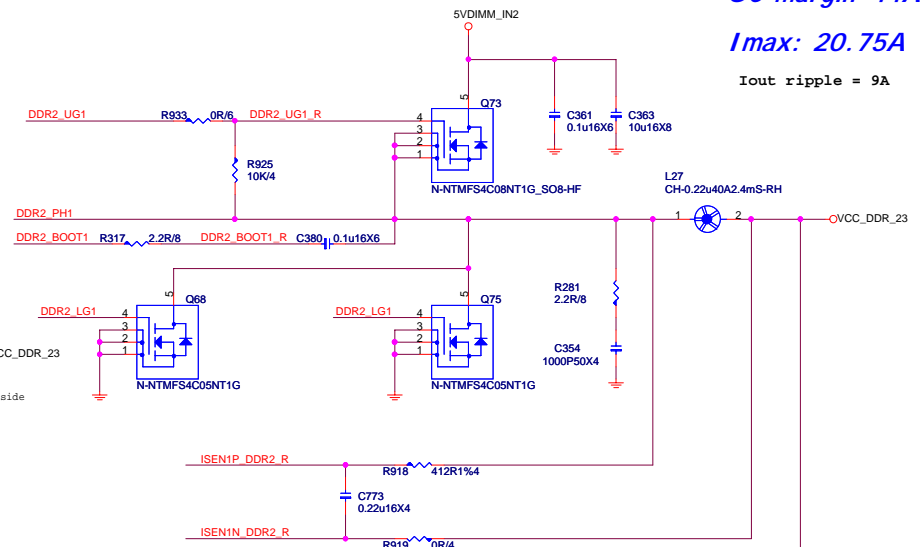
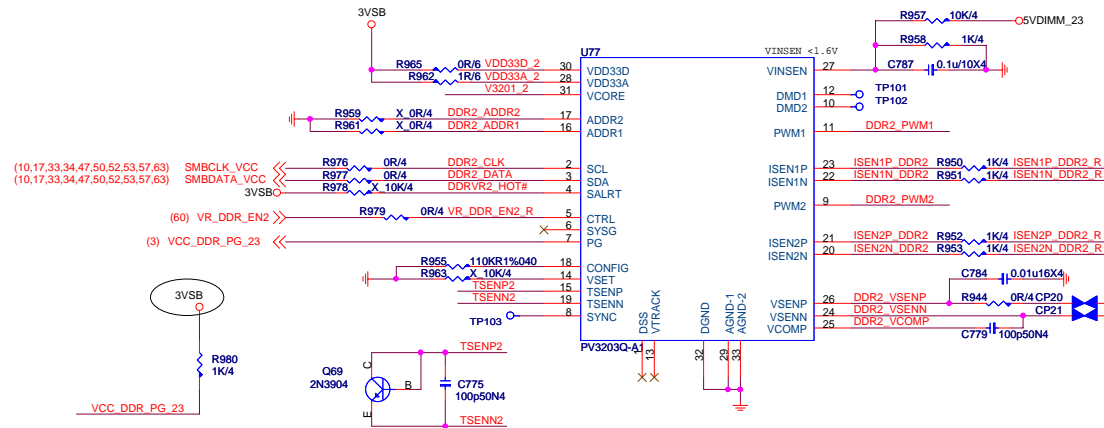
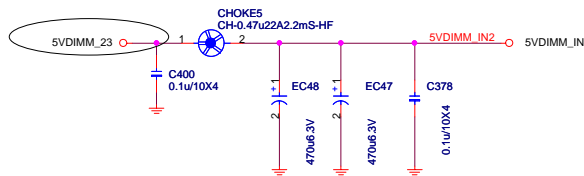
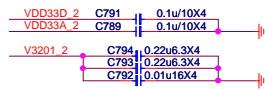
Iin ripple = 5.082A

OCP=64A

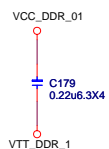
OC margin=44A

I<sub>max</sub>: 20.75A

I<sub>out</sub> ripple = 9A



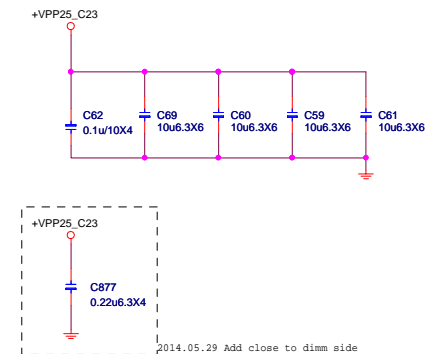
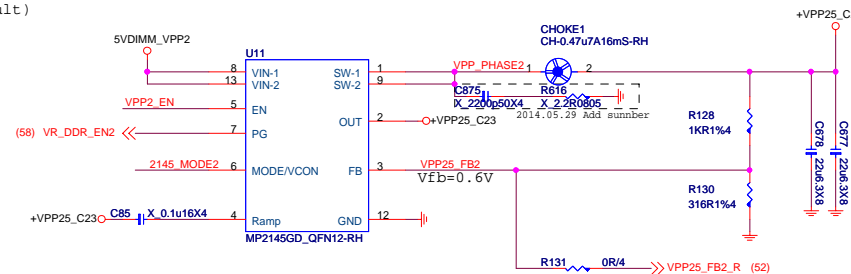
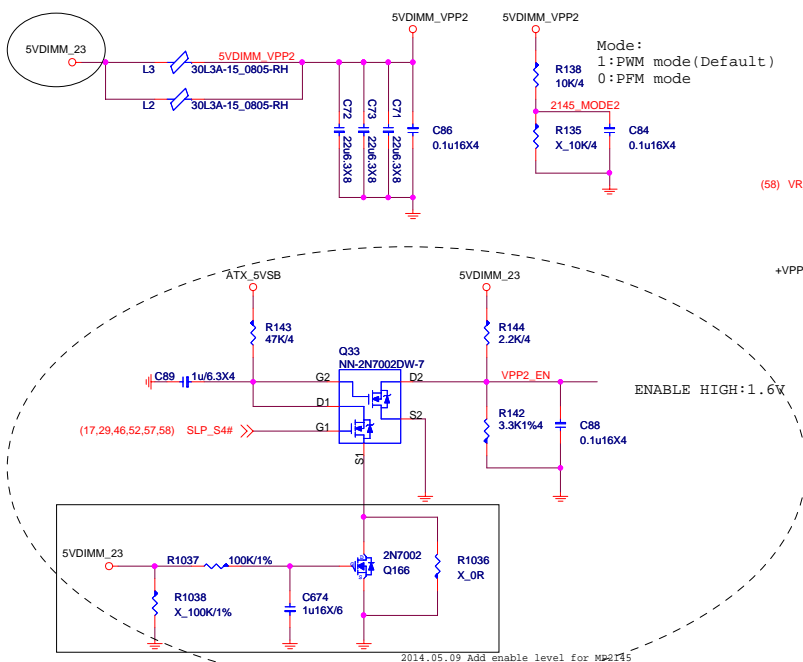
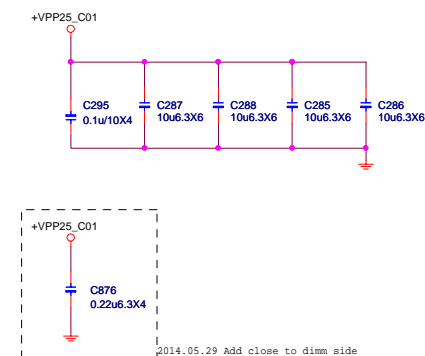
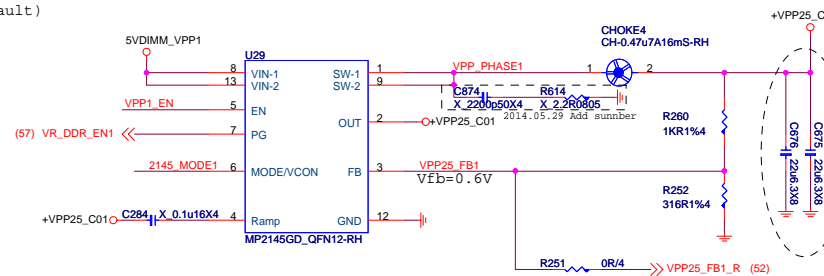
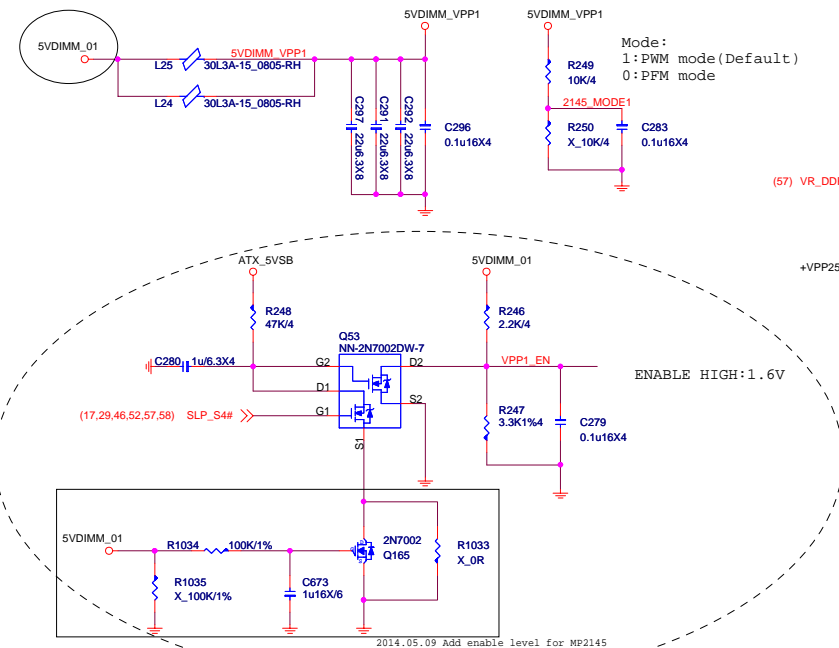
*4DIMM :3A FOR OC margin*



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# 4DIMM :6A FOR DDR VPP



*PCH Core 6.504A*

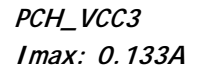
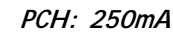


\_\_\_\_\_

MAX 10A  
ILIMIT=10A~12A 峰谷



Waitting PCH\_1P05 Ready



*C854 close to PCH*

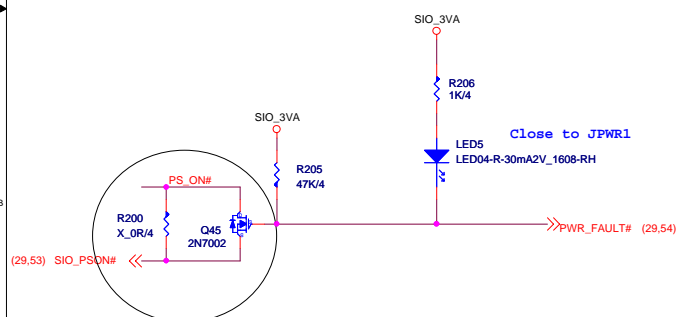


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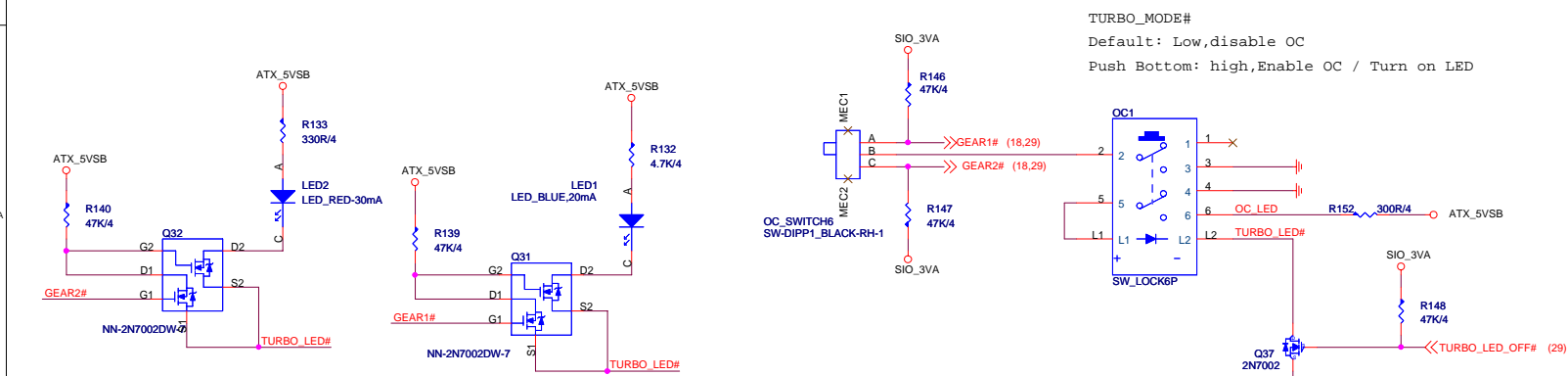
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[illegible][illegible]

Pin 19 to 28 of the H2XT10JM-2PITCH package. The diagram shows a 10-pin connector with pins numbered 1 to 10. Pin 1 is TPM\_CLK (19,63). Pin 2 is TPM\_RST# (29). Pin 3 is LPC\_ADO (17,29). Pin 4 is LPC\_AD0 (17,29). Pin 5 is LPC\_AD1 (17,29). Pin 6 is LPC\_AD2 (17,29). Pin 7 is LPC\_AD3 (17,29). Pin 8 is LPC\_FRAME# (17,29). Pin 9 is JTPM1 (3VSB). Pin 10 is VCC3 (VCC3). Pin 11 is SERIRQ (SERIRQ). Pin 12 is OVCCS (OVCCS). Pin 13 is H2XT10JM-2PITCH.



VCCP

VCC\_DDR\_01

VCC\_DDR\_23

+VPP25\_C01

+VPP25\_C23

CPU\_CORE3

PCH\_1P05

C112 10uF 3X/6V

C103 10uF 3X/6V

C97 10uF 3X/6V

C94 10uF 3X/6V

C82 10uF 3X/6V

C91 10uF 3X/6V

PWRCONNP\_BLACK-RH-4

1

2

3

4

5

6

7

8

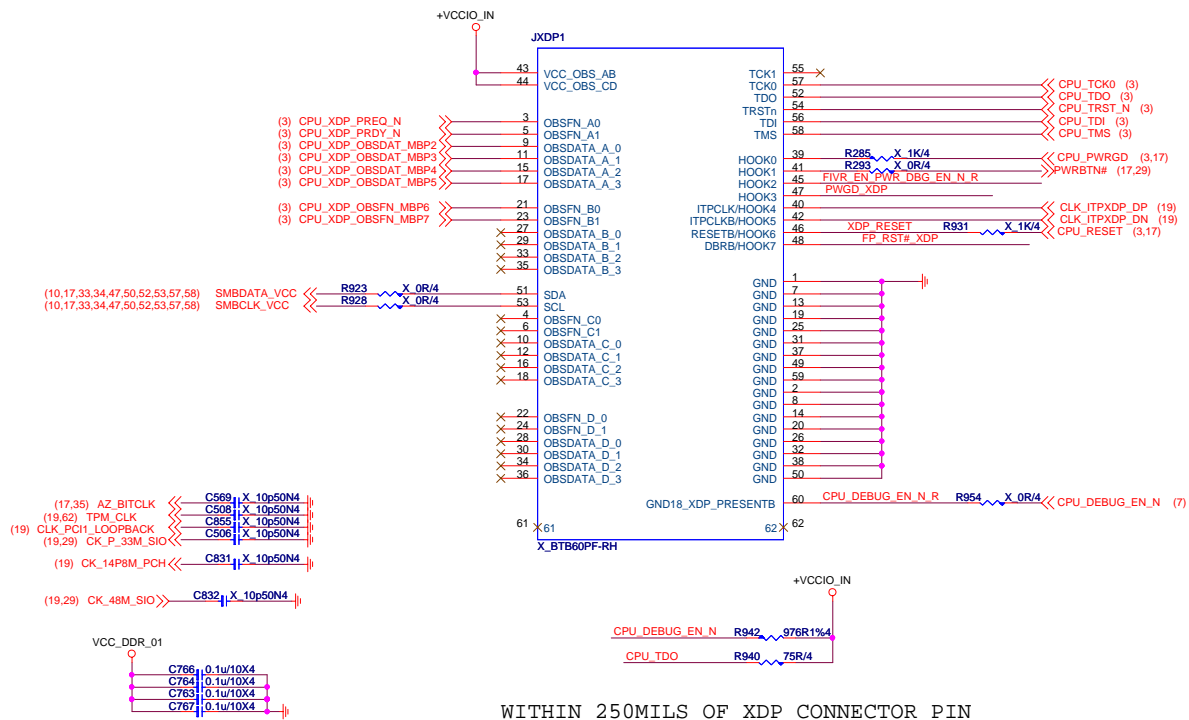
9



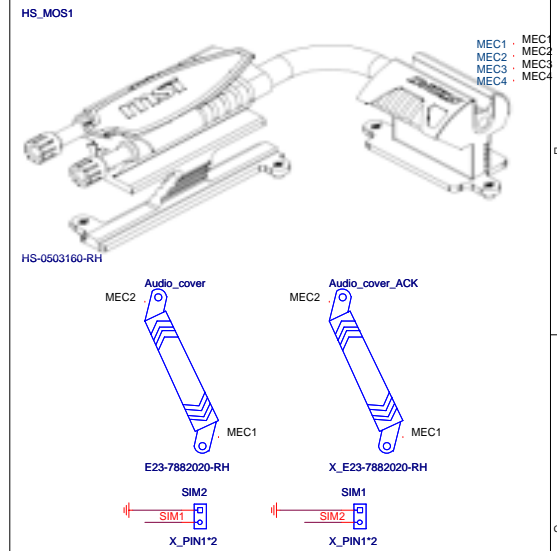
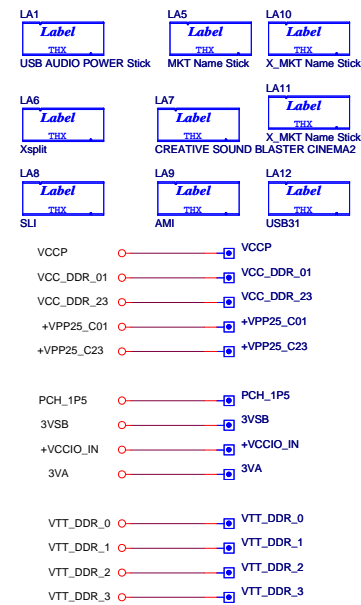
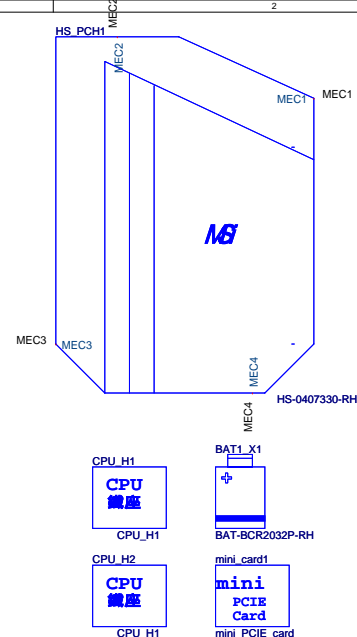
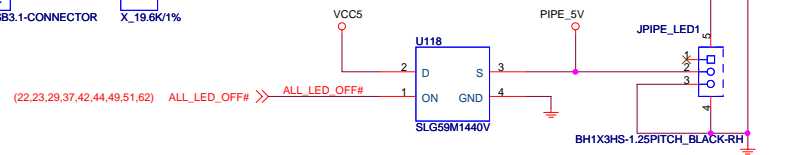
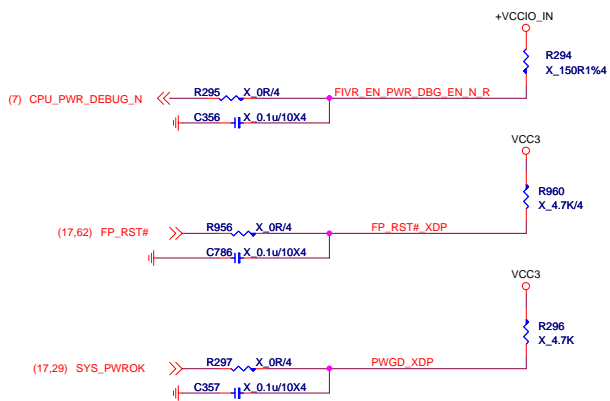
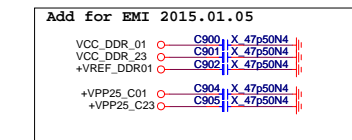
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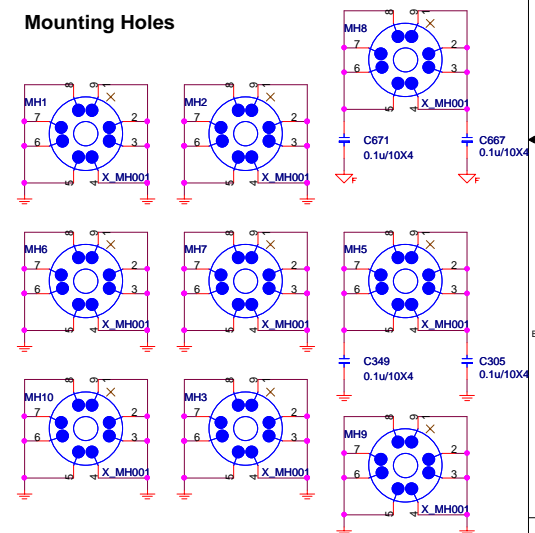
**Reserve debug port 5020**



WITHIN 250MILS OF XDP CONNECTOR PIN



## Mounting Holes



### Optical Fiducial Marks-120

